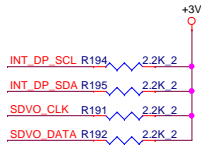
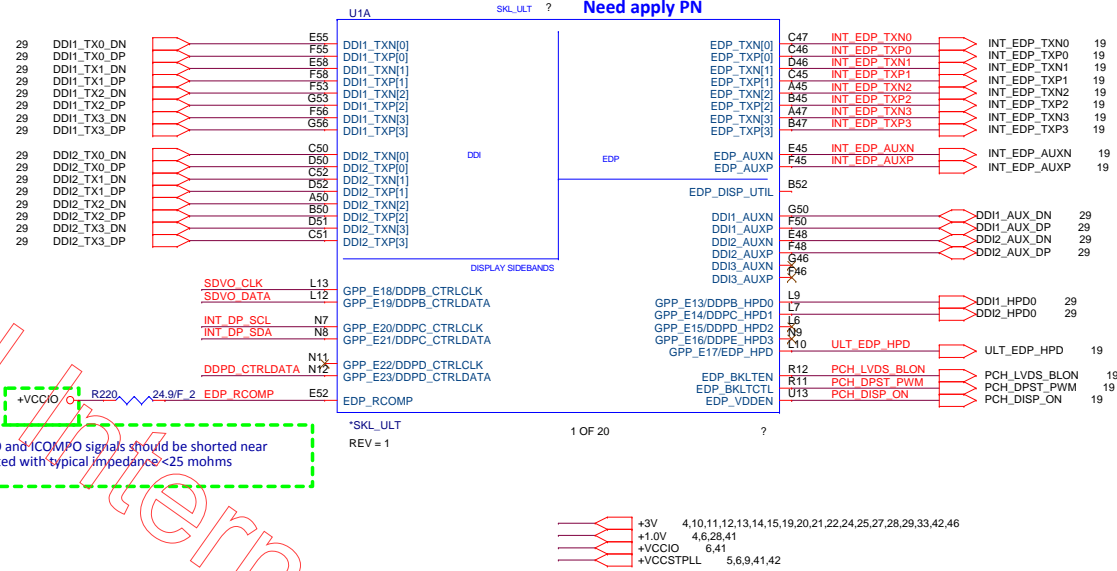
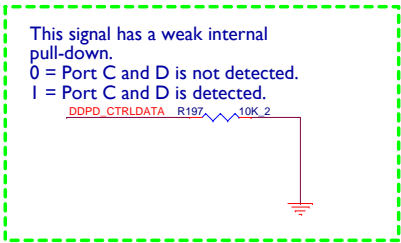


01

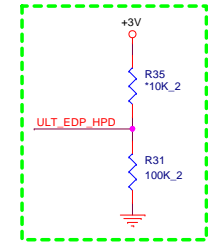




DDPB_CTRLDATA/ GPP_E19
Display Port B Detected
This signal has a weak internal pull-down.
0 = Port B is not detected.
1 = Port B is detected.



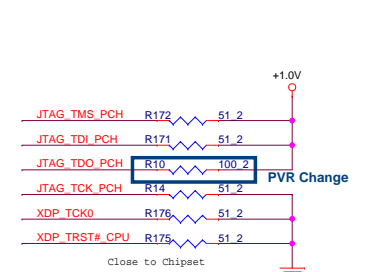
Reserve EDP_HP0 opposites circuit!



eDP_COMPIO and ICOMPIO signals should be shorted near balls and routed with typical impedance <25 mohms

Close to EC

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL
470 OHM IS FOR I/P

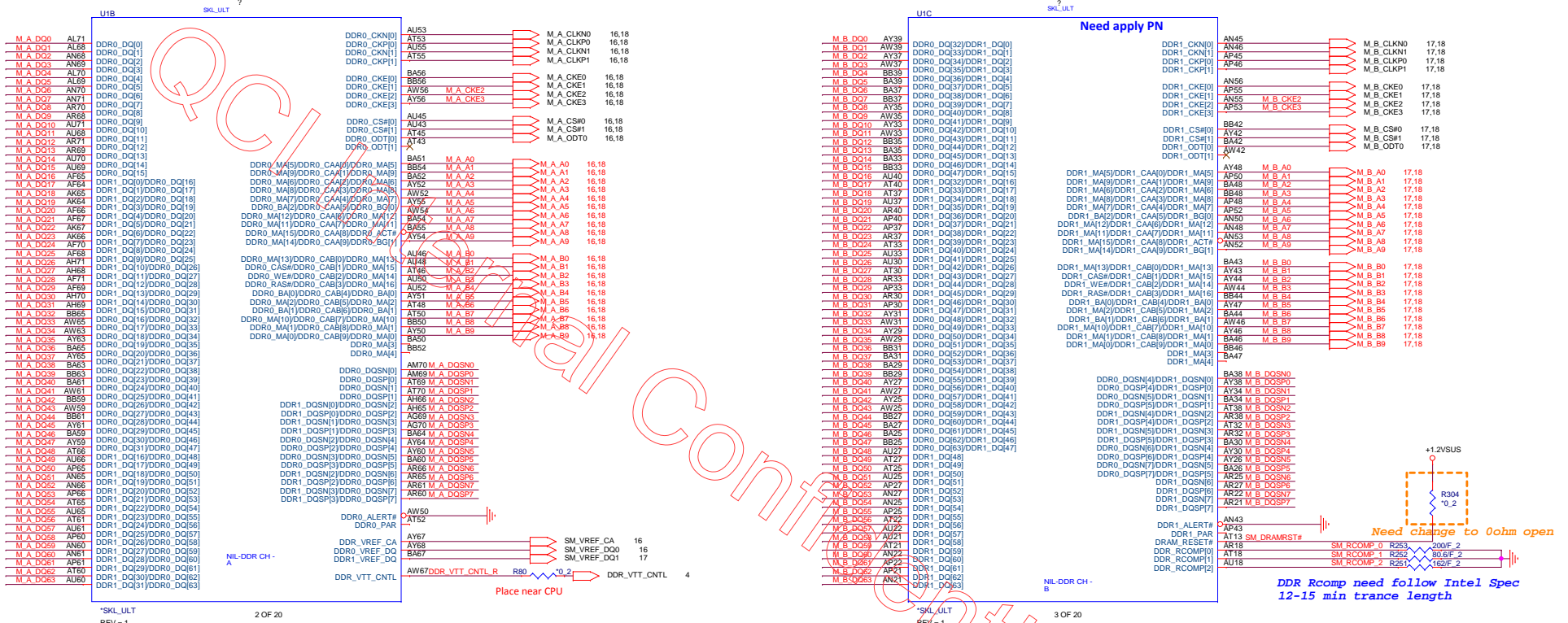


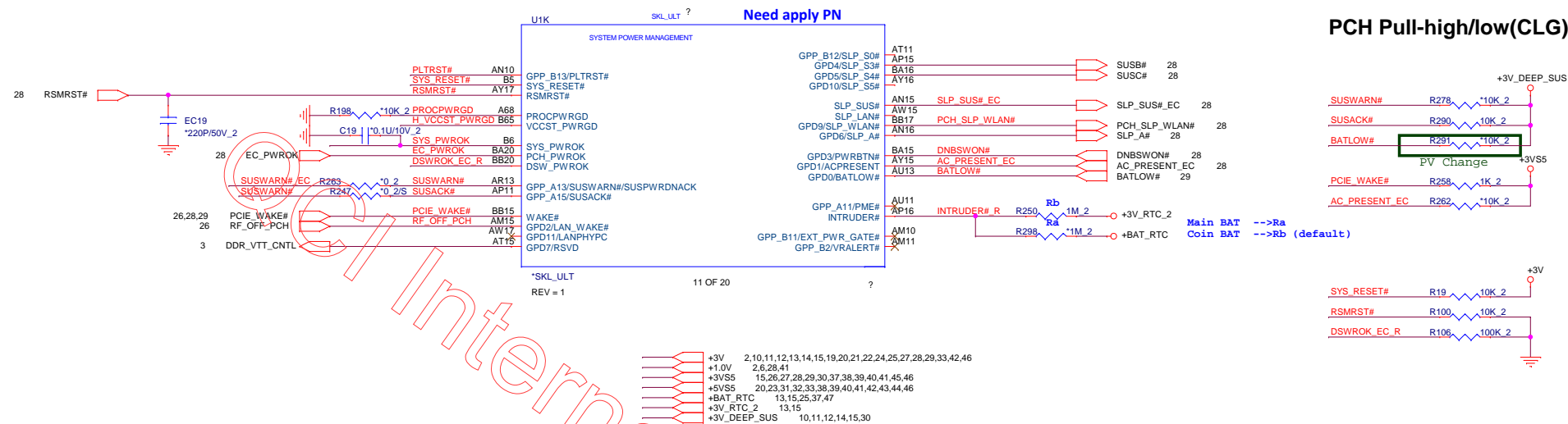
PROJECT : X31
Quanta Computer Inc.

Size	Document Number	Rev
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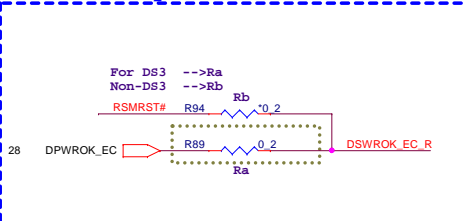
KABYLAKE ULT Processor LPDDR3 x32

Need apply PN

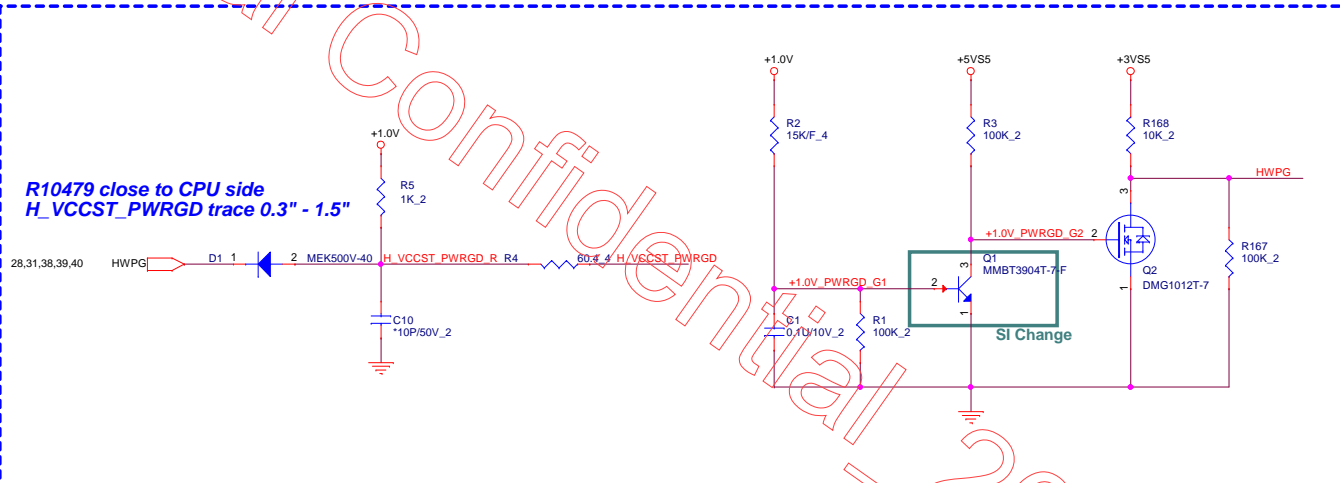




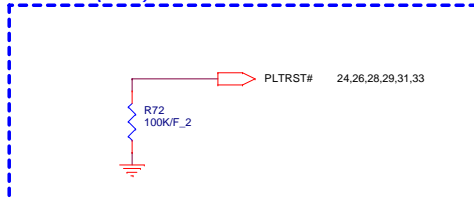
For DS3 Sequence



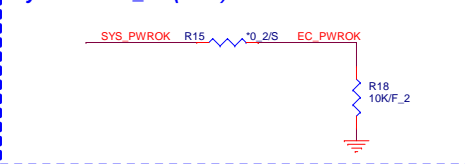
HW Power Good Circuit

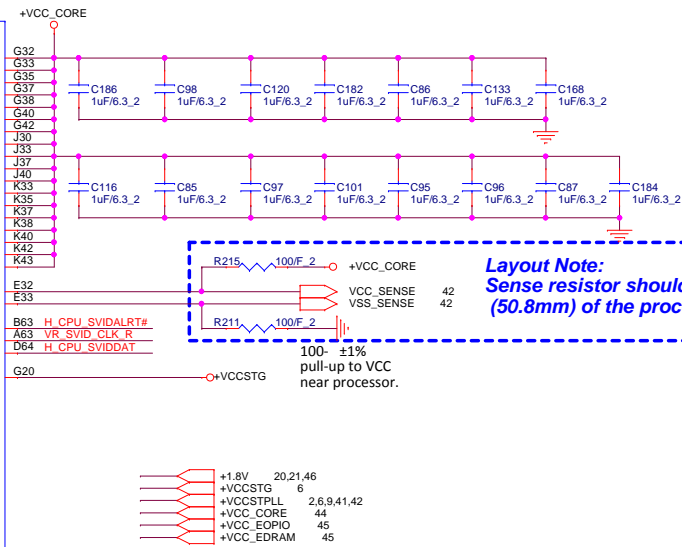
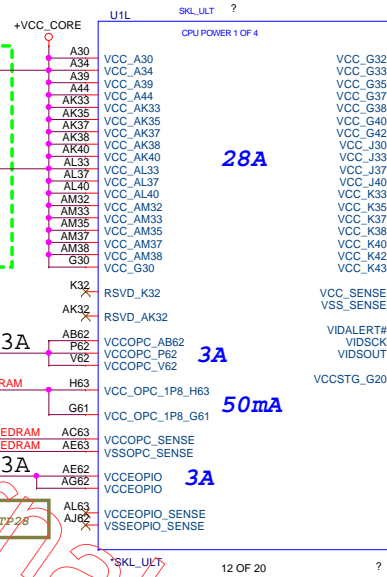
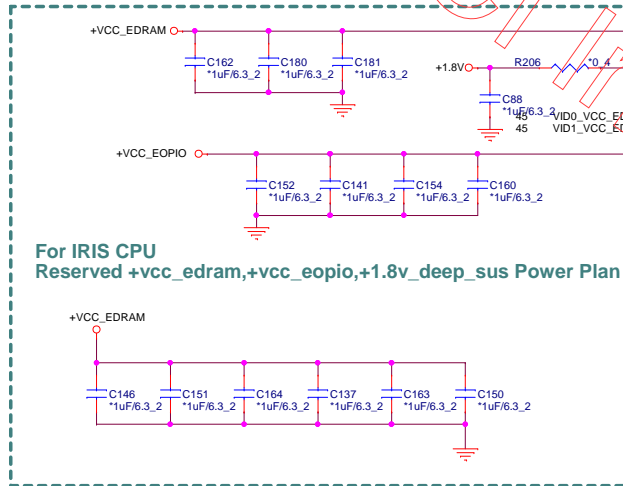
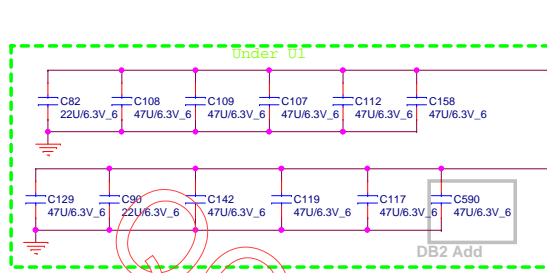


PLTRST#(CLG)



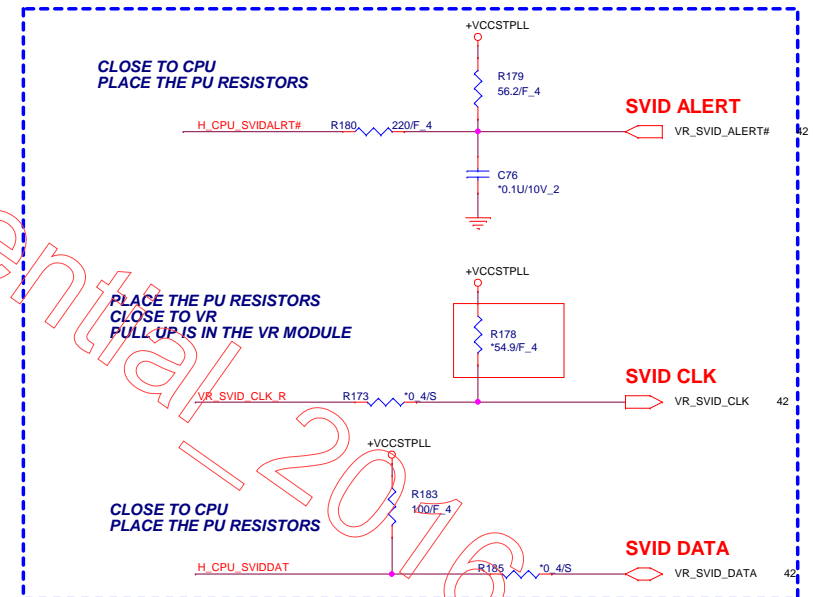
System PWR_OK(CLG)






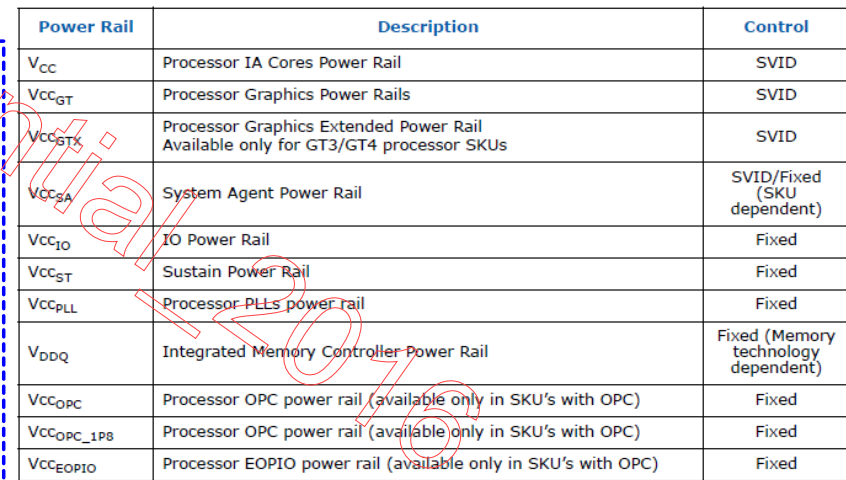
+1.8V	20,21,46
+VCCSTG	6
+VCCSTPLL	2,6,9,41,42
+VCC_CORE	44
+VCC_EOPIO	45
+VCC_EDRAM	45

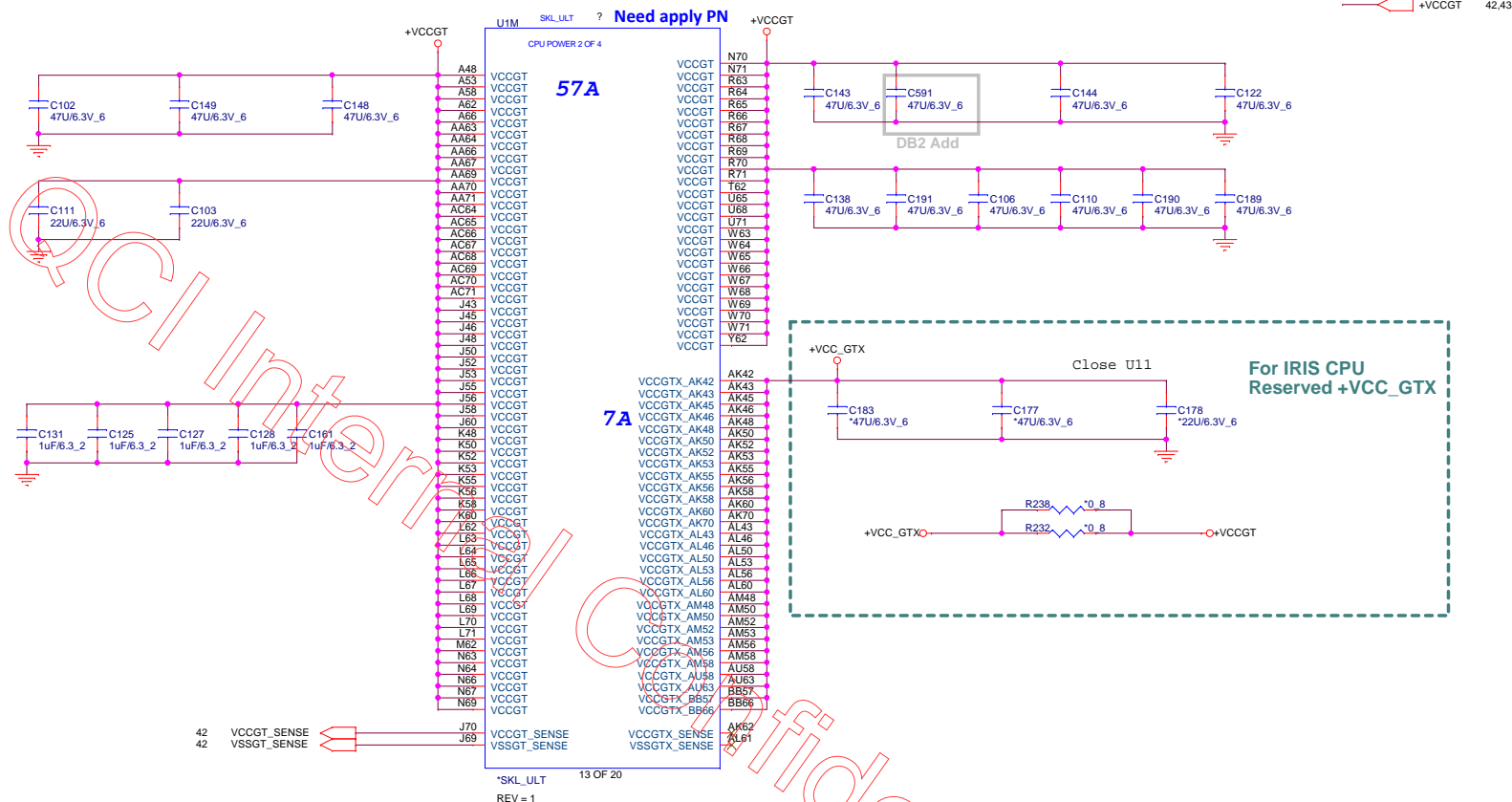
Layout note: need routing together and ALERT need between CLK and DATA.




Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

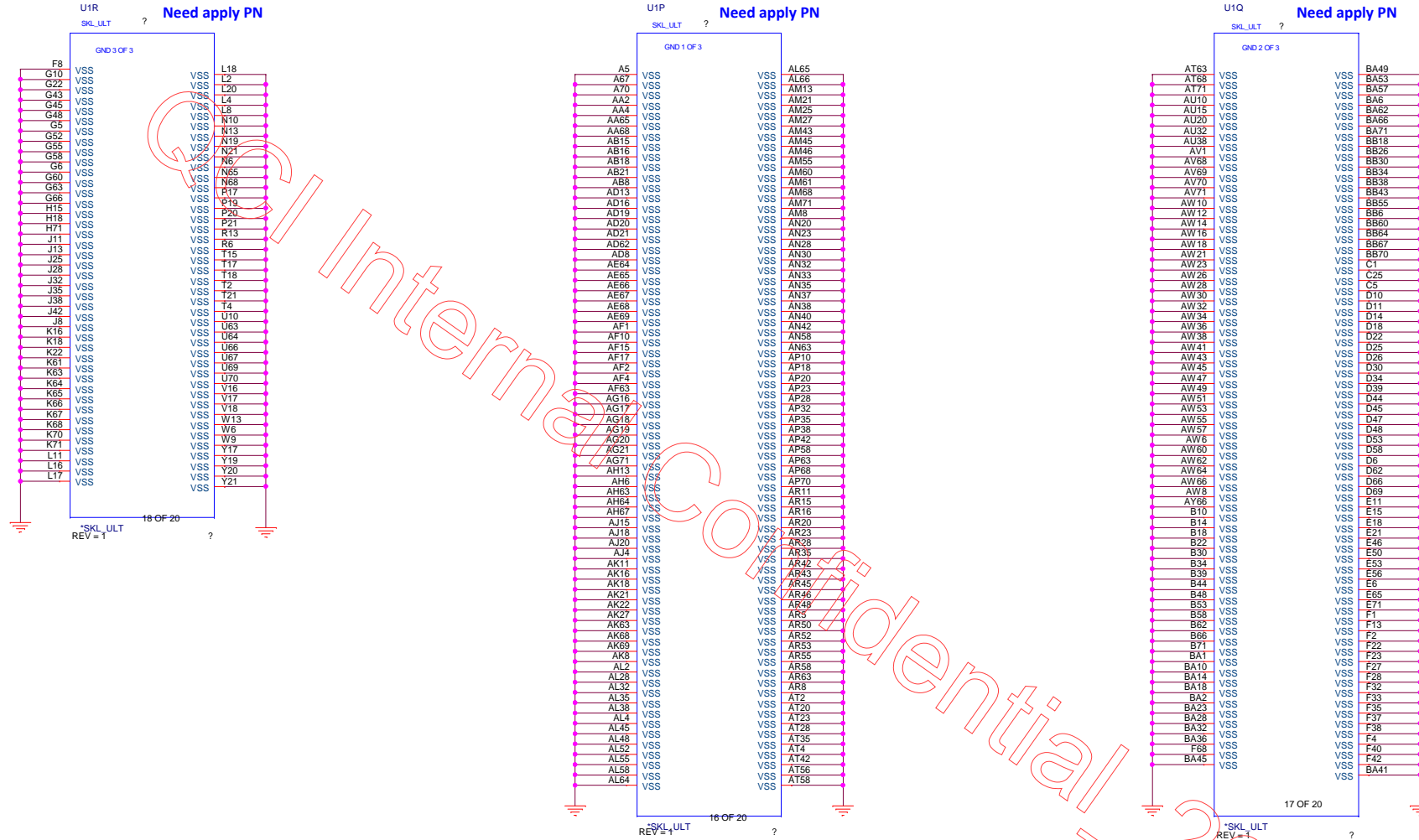
 NB5		PROJECT : X31 Quanta Computer Inc.		
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Date: Friday, August 05, 2016		Sheet 5 of 49		

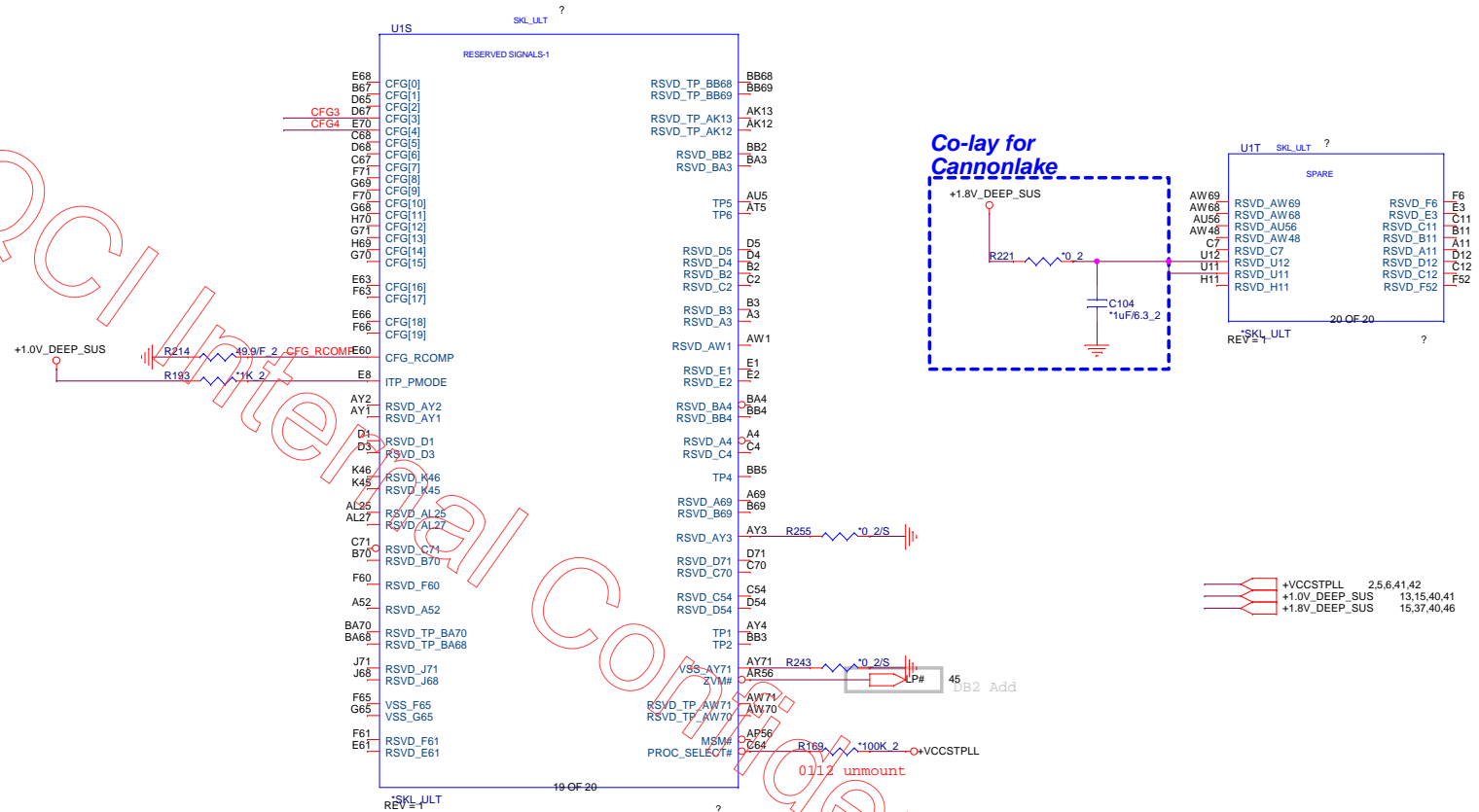




Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

			PROJECT : X31 Quanta Computer Inc.		
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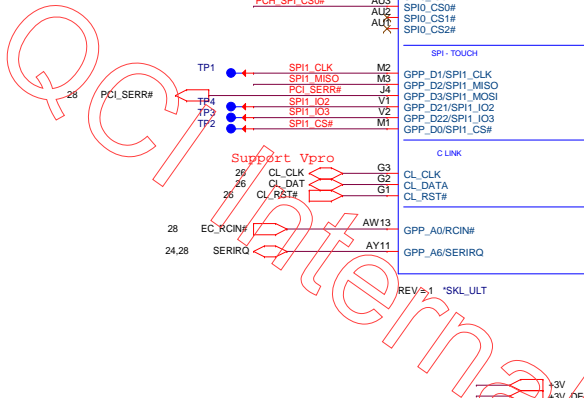




Processor Strapping

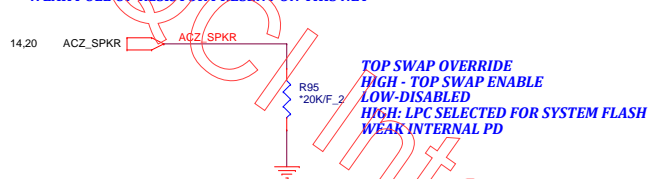
The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R199 *1K 2
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R204 *1K 2

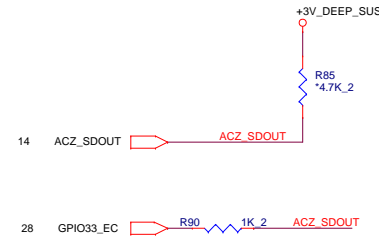


Functional Strap Definitions

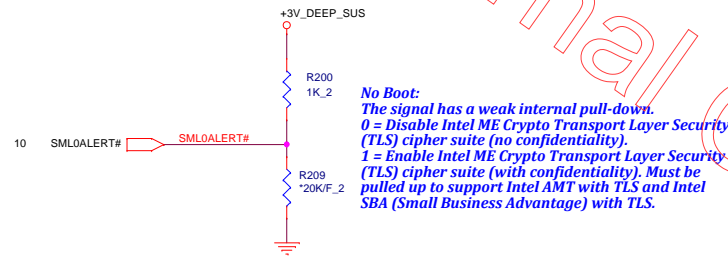
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



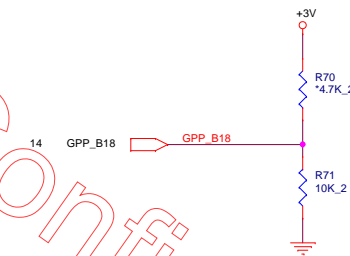
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



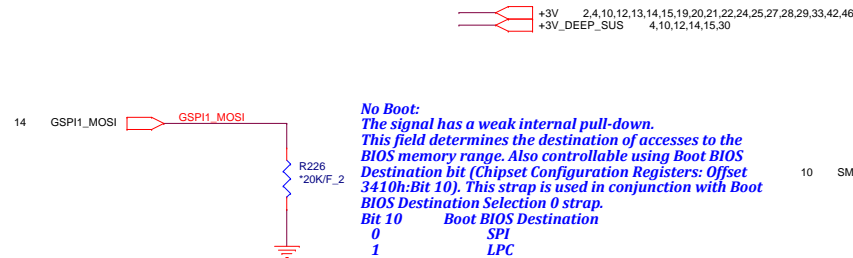
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



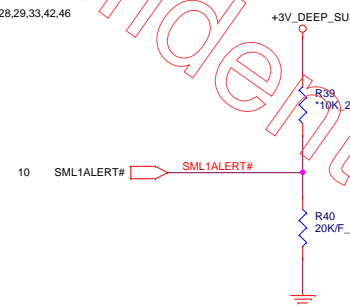
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.




No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

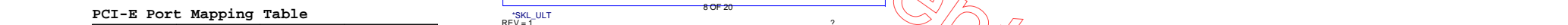


No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

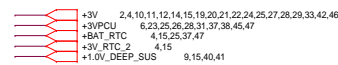
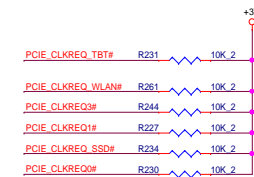
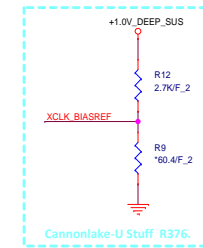
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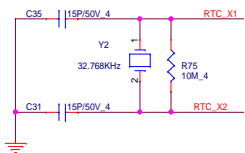
PCI-E Port	Function	CLK RQ Port	Function
Port1	Un-used	Port0	Un-used
Port2	WLAN	Port1	Un-used
Port3	Un-used	Port2	WLAN
Port4	Un-used	Port3	Un-used
Port5	Thunderbolt	Port4	Thunderbolt
Port6	Thunderbolt	Port5	SSD HDD
Port7	Thunderbolt		
Port8	Thunderbolt		
Port9	SSD HDD		
Port10	SSD HDD		
Port11	SSD HDD		
Port12	SSD HDD		

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	NC
PORT-3	NC
PORT-4	NC

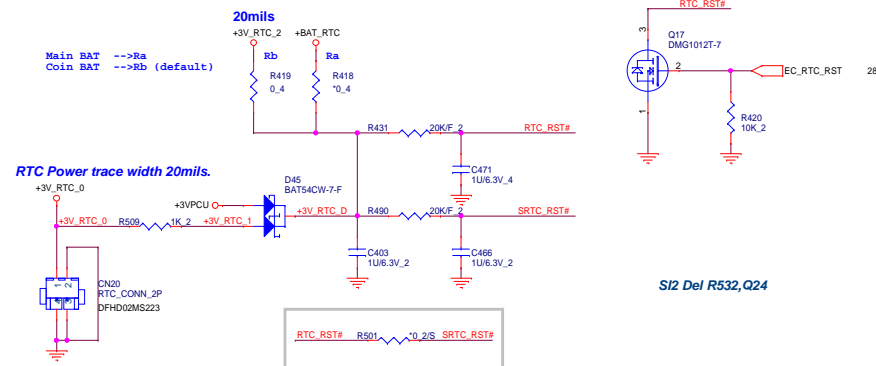
USB2.0	Function
PORT-1	USB3.0 MB-1
PORT-2	NC
PORT-3	NC
PORT-4	NC
PORT-5	HD Camera
PORT-6	IR Camera
PORT-7	WLAN
PORT-8	OLED Touch Screen
PORT-9	NC
PORT-10	NC



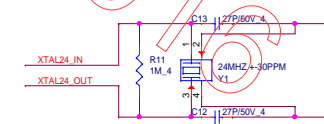
RTC Clock 32.768KHz

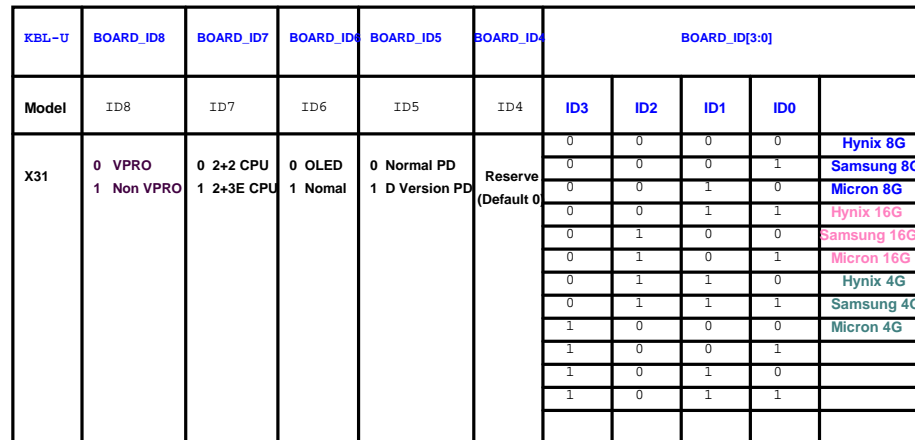


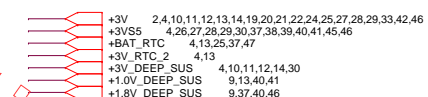
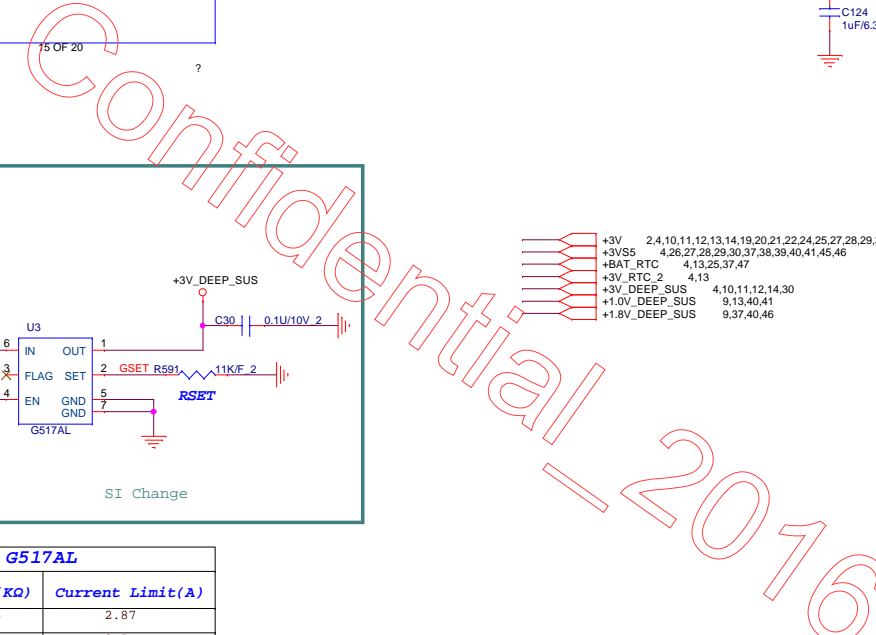
RTC Circuitry(RTC)



External Crystal







G517AL	
RSET(KΩ)	Current Limit(A)
9.76	2.87
11	2.5
24.9	1.0
37.4	0.7
49.9	0.5
100	0.25

Channel A:4Gb/8Gb/16Gb*2 LPDDR3-1866

4G Main Memory Configurable

AKD5RW0TW44, IC SDRAM(178)H9CCNN8JTLAR-NUD TOPB8Q
AKD5QWST523, ICSDRAM(178P)K4E8E304EB-BGCF(FBGA)TOPB8Q
AKD5QWSTL05, IC SDRAM178P MT52L256M32D1PF-107 TOPB8Q

8G Main Memory Configurable

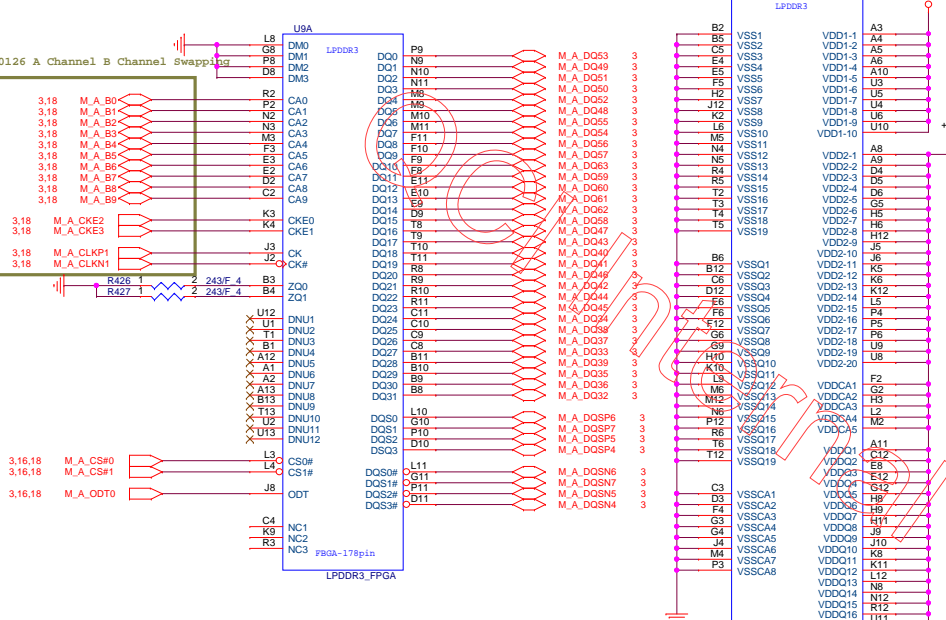
AKD5RW0TW42, IC SDRAM(178)H9CCNN8JTLAR-NUD TOPB8Q
AKD5RZST503, IC SDRAM(178P)K4E8E304EB-BGCF TOP B8Q
AKD5RWSTL05, IC SDRAM178P MT52L256M32D2PF-107 TOPB8Q

16G Main Memory Configurable

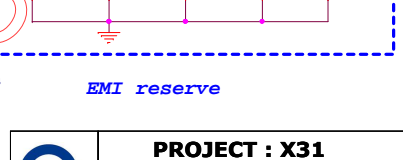
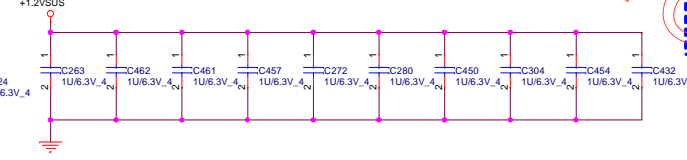
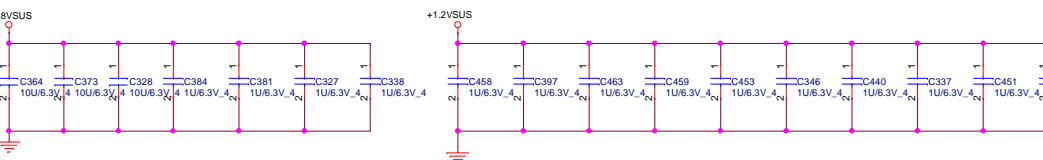
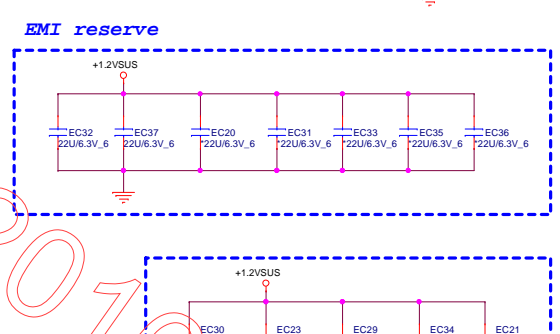
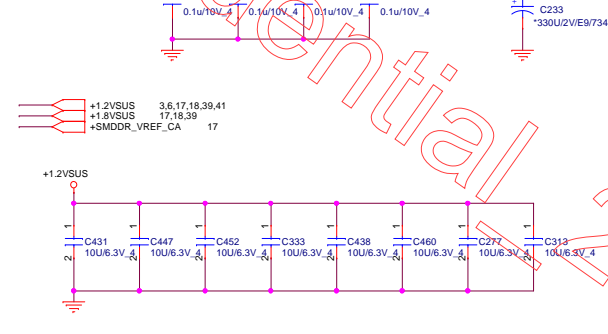
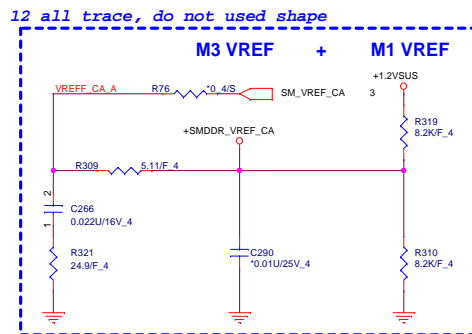
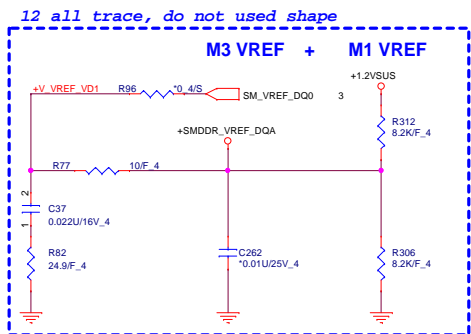
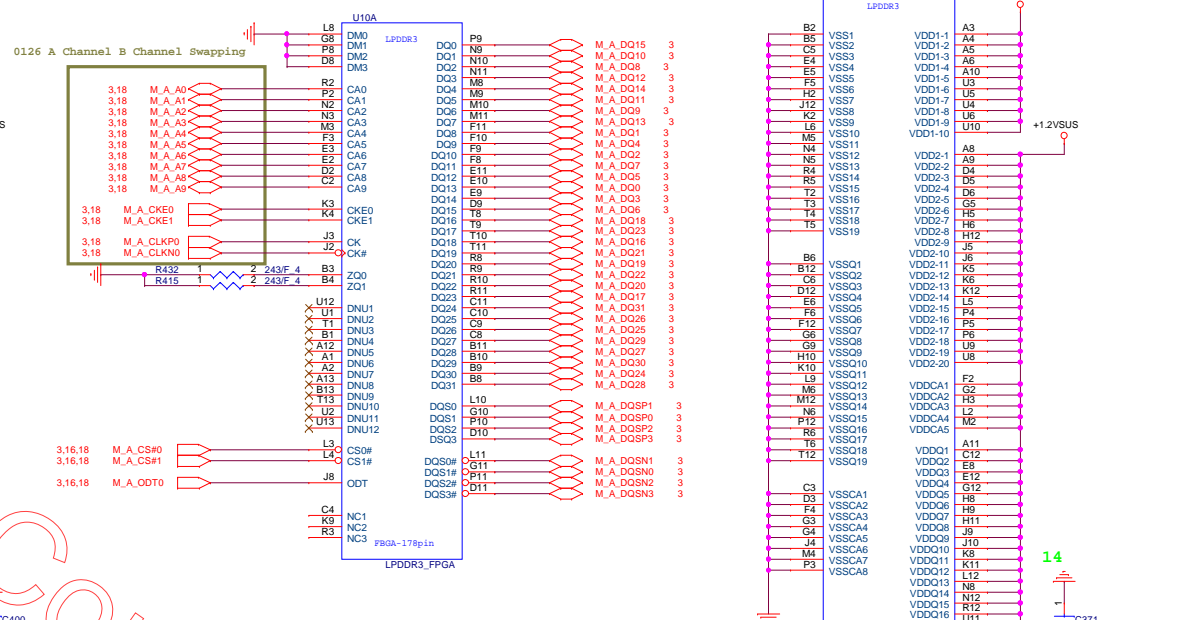
AKD5RW0TW22, IC SDRAM(178) H9CCNNCLTTLAR-NUD TOP B8Q
AKD5P2ST507, ICSDRAM(178P)K4E8E304EB-BGCF(FBGA)TOPB8Q
AKD5RWSTL02, IC SDRAM(178P)MT52L1G32D4PG-107 TOP B8Q

16

bit:32-63



bit:0-31



I'm from VIETNAM sualaptop365

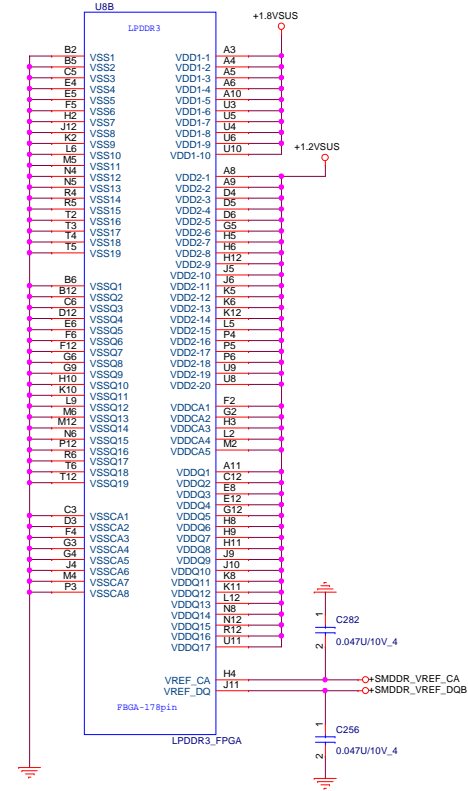
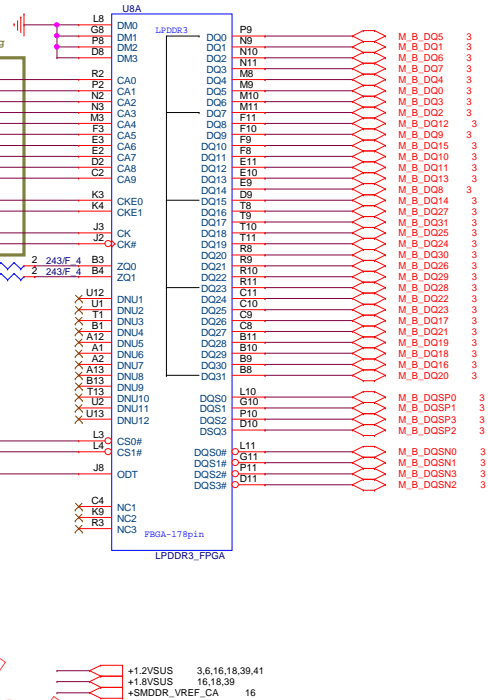
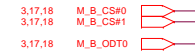
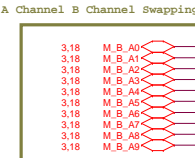
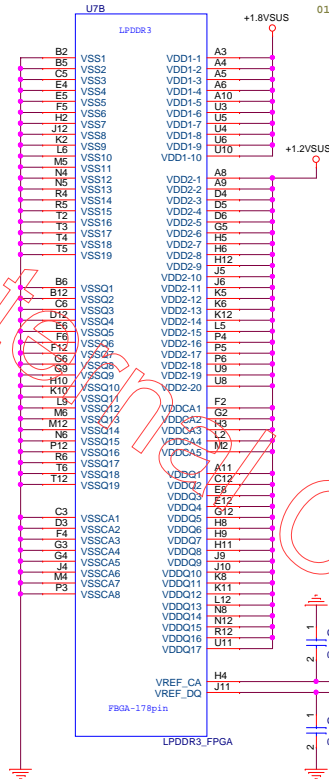
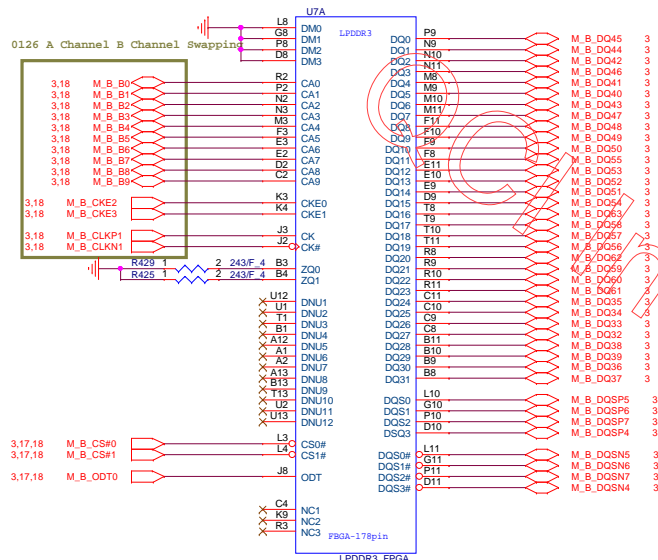
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Quanta Computer Inc.

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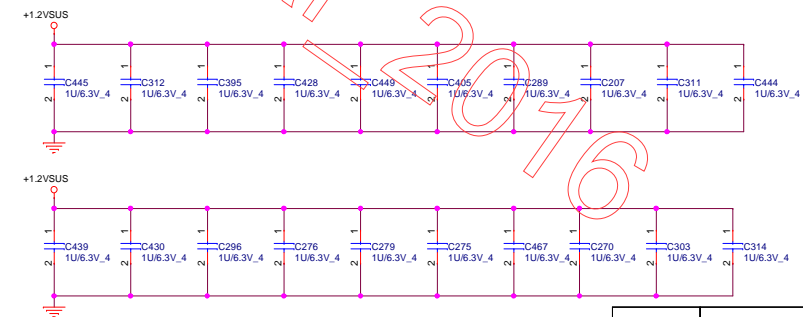
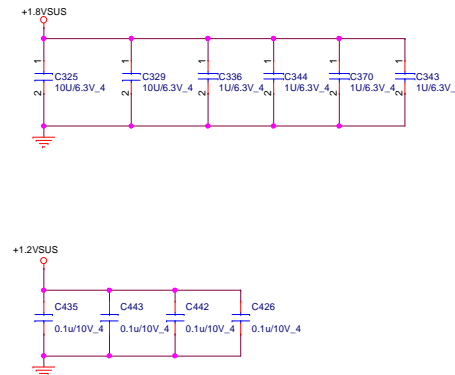
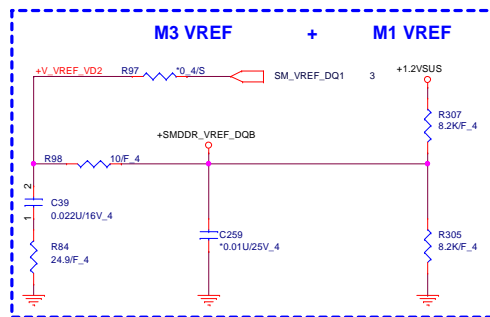
CHANNEL B:4Gb/8Gb/16Gb*2 LPDDR3-1866

4G Main Memory Configurable	8G Main Memory Configurable	16G Main Memory Configurable	
AKD5RW0T44, IC SDRAM(178)H9CCNN80BTMLAR-NUD TOPBSQ	AKD5RW0T42, IC SDRAM(178)H9CCNN80BTMLAR-NUD TOPBSQ	AKD5RW0T22, IC SDRAM(178) H9CCNNCLTMLAR-NUD TOP BSQ	Hynix
AKD5QMS753, ICSDRAM(178P)K4BE304BEE-EGCF(FBGA)TOPBSQ	AKD5SZT503, IC SDRAM(178P)K4BE304BEE-EGCF TOP BSQ	AKD5PZT507, ICSDRAM(178P)K4BE304BEE-EGCF(FBGA)TOPBSQ	Samsung
AKD5QMSLT05, IC SDRAM178P MT52L256M32D1PF-107P TOPBSQ	AKD5RWDLT05, IC SDRAM178P MT52L512M32D2PF-107P TOPBSQ	AKD5SWLT02, IC SDRAM(178P)MT52L1G32D4PG-107 TOP BSQ	Micron

bit:32-63

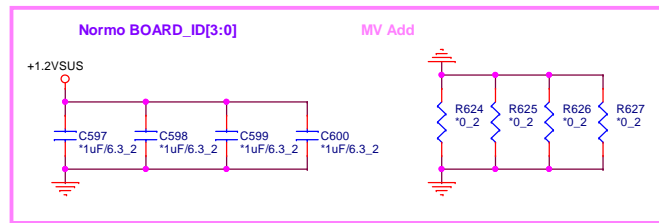
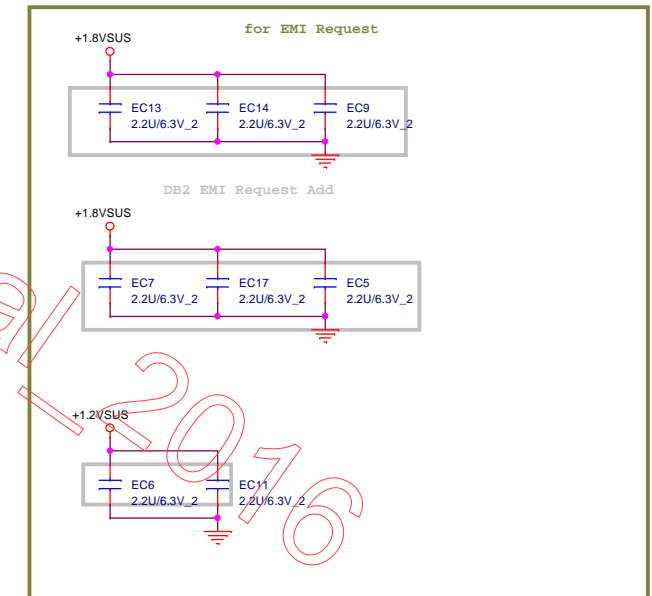
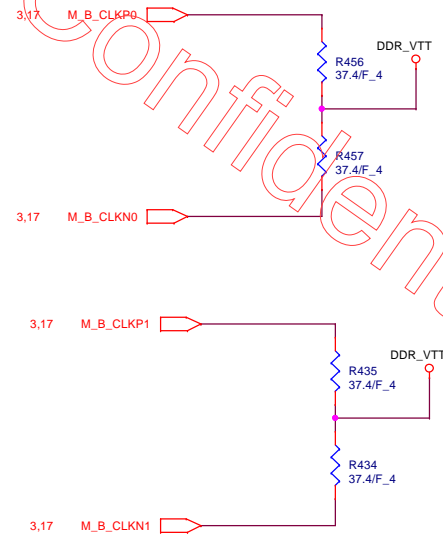
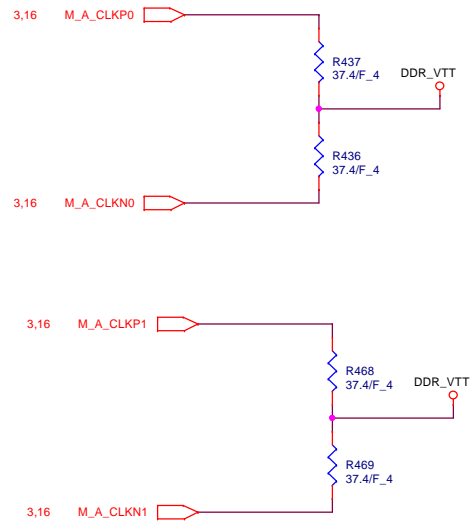
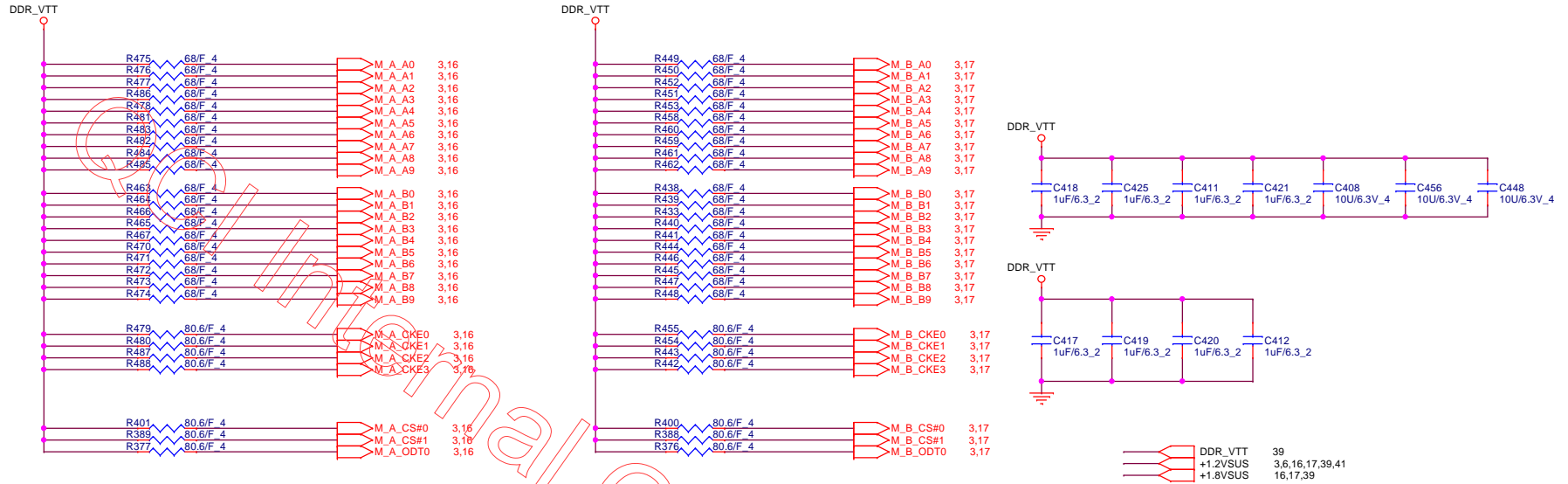


12 All 20mil trace, please do not use shape



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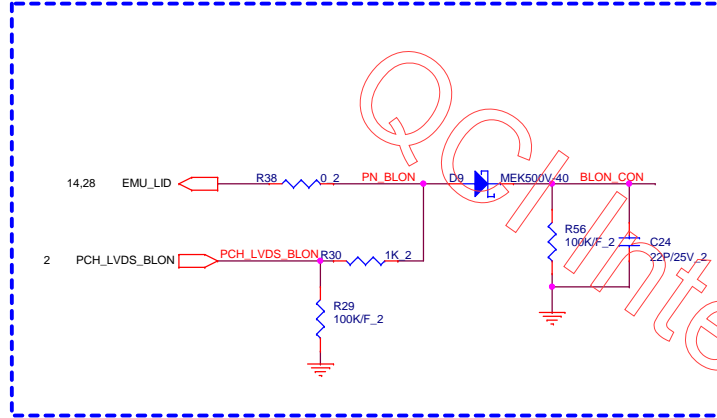
Size	Document Number LPDDR3 B	Rev 1A
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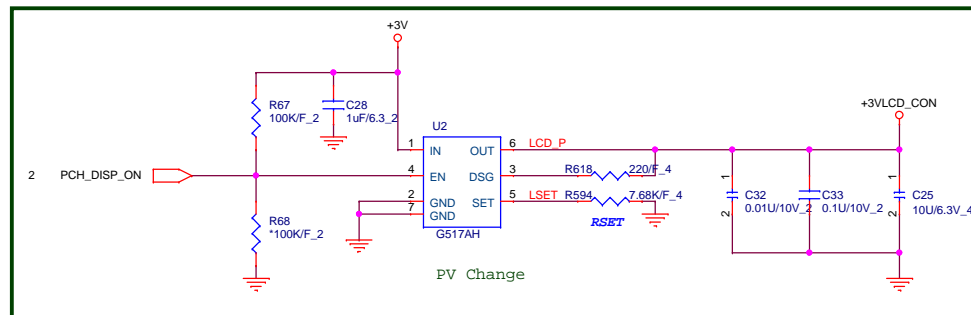
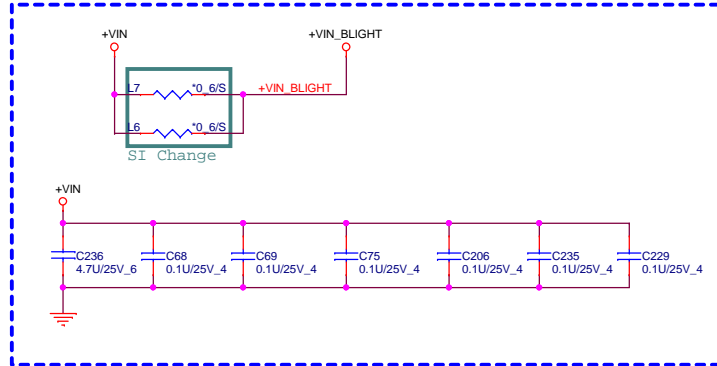
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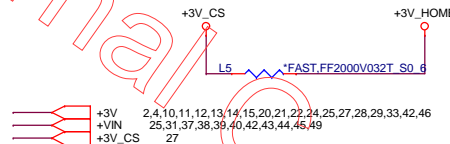
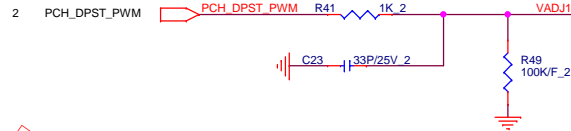
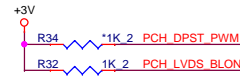
LID Switch



Panel Vin Cap

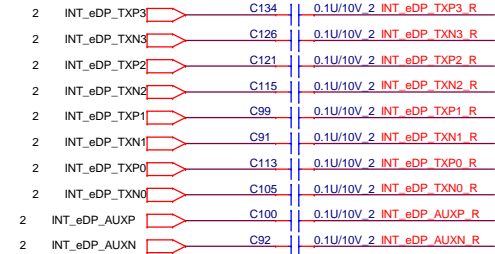
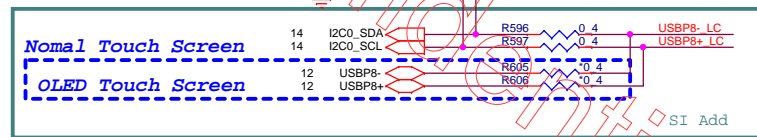


G517AH	
RSET(KQ)	Current Limit(A)
7.68	2.7
10.5	2
21	1
42	0.5

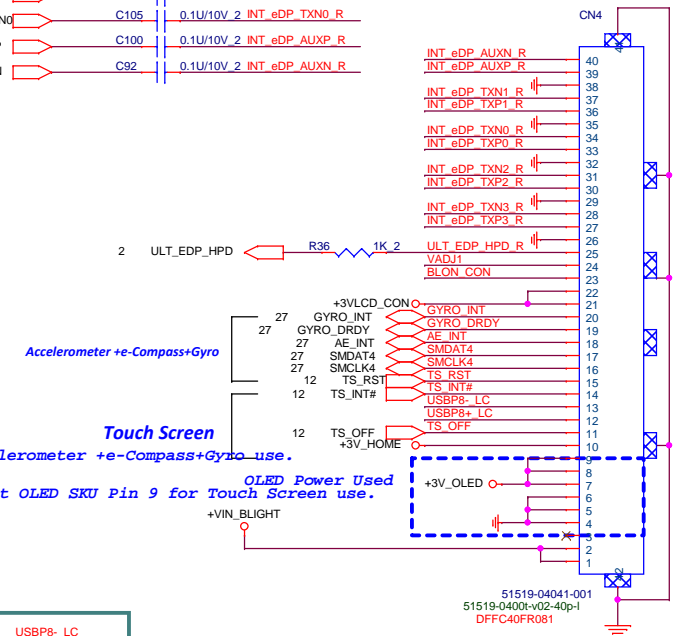


Normal Touch Screen

OLED Touch Screen



eDP Conn.



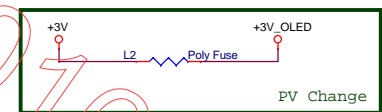
Touch Screen

No support OLED SKU Pin 9 for Touch Screen use.

Poly Fuse

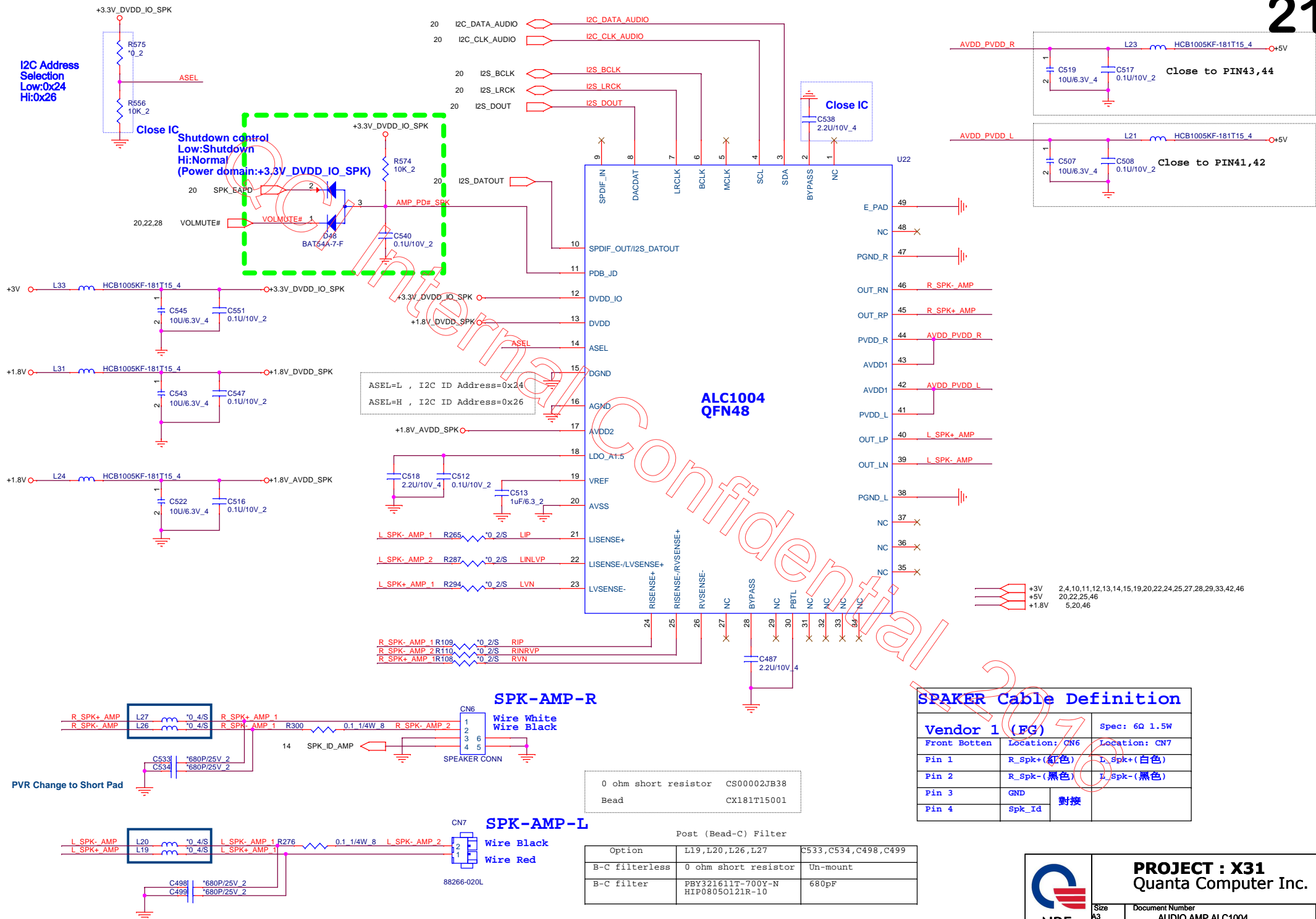
Vender	Size	P/N
WYN	0805	DK150TPU025 (LP-ISML150)
LFI	0805	DK150TPU022 (0805L150ULYR)
PYS	0805	DK150TPU018 (SPR-P150)

OLED Power Used

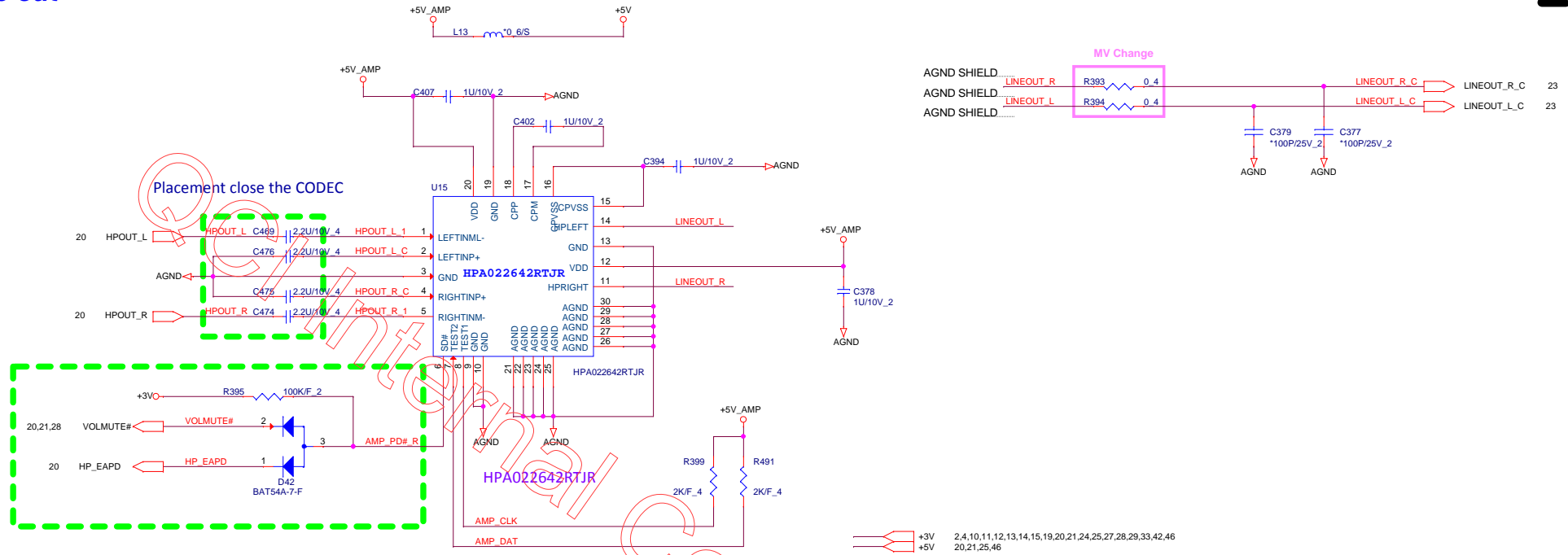


PROJECT : X31
Quanta Computer Inc.

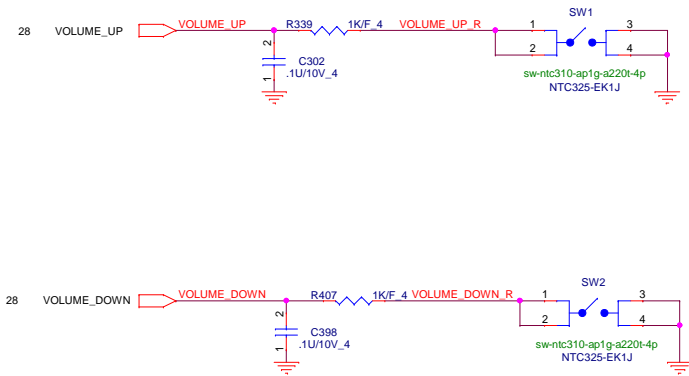
Size	Document Number	Rev
Custom	LCD CONN/CAM/LID	
Date: Friday, August 05, 2016	Sheet 19 of 49	



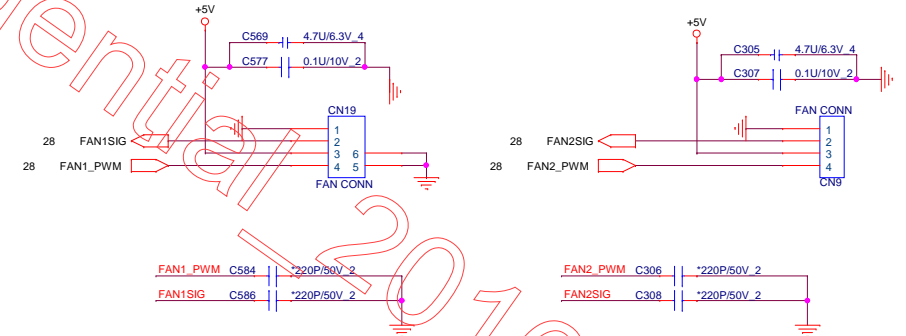
Head Phone out



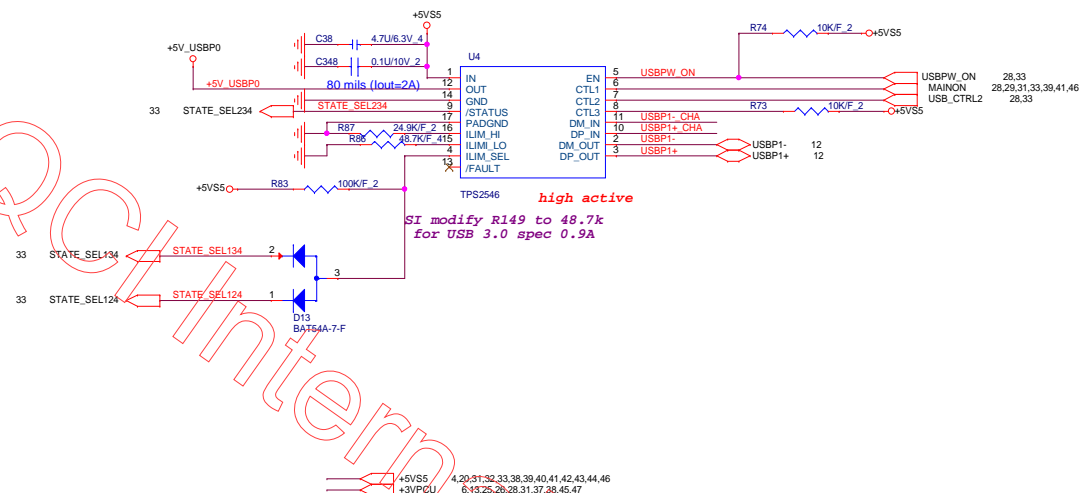
Volume up/down Button



FAN

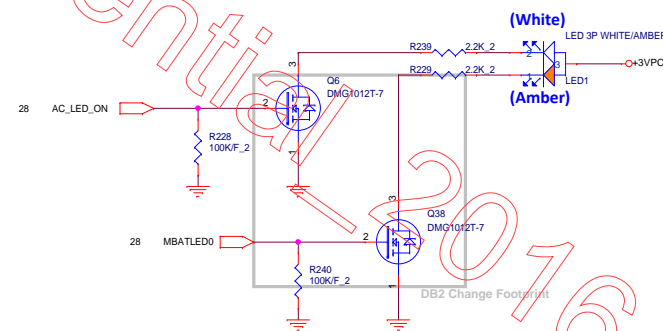
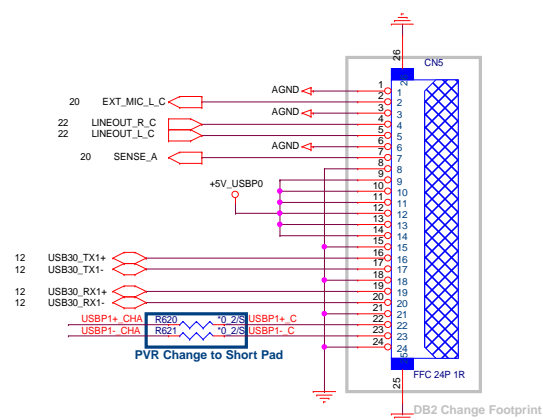


	PROJECT : X31		
	Quanta Computer Inc.		
Size Custom	Document Number	Rev	
AUDIO AMP/FAN/Volume Button			
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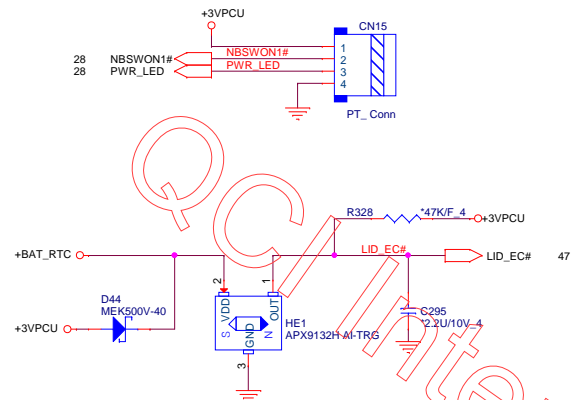


AUdio Combo Jack + USB3.0 Daughter Board

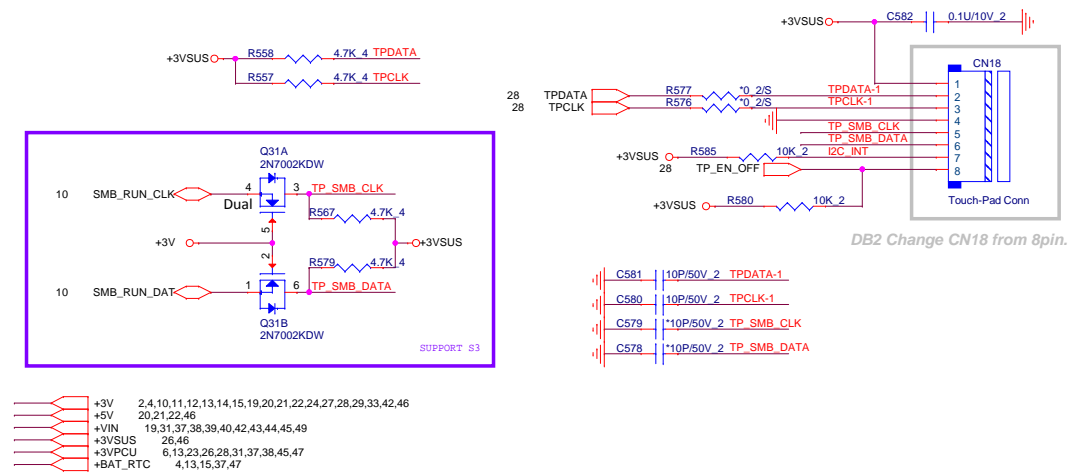
AC IN / BATTERY LOW LED



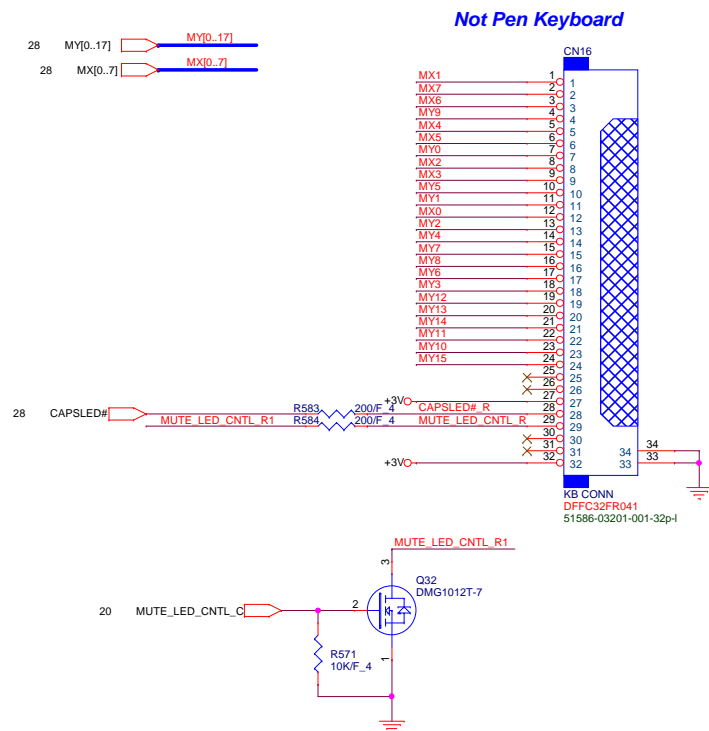
Power Button Connector and LID



Touch Pad Connector

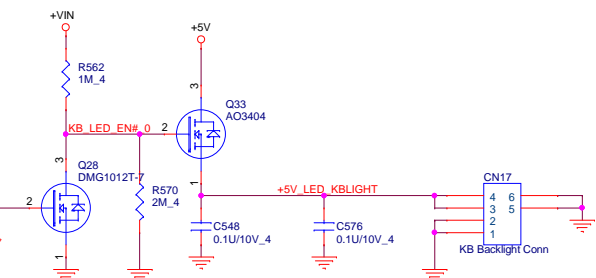
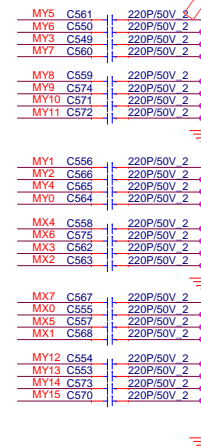


KEYBOARD Con Co-Lay

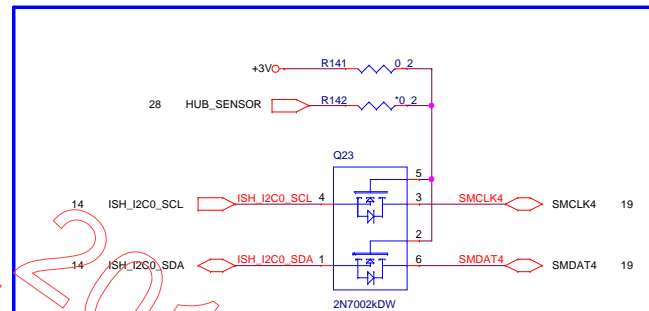
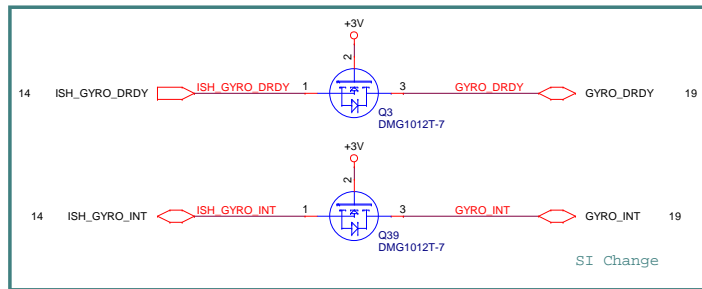
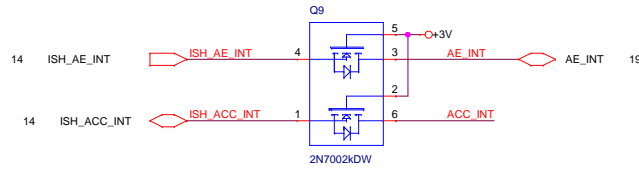
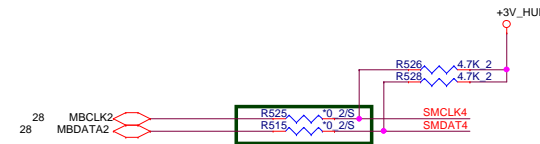
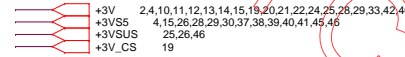
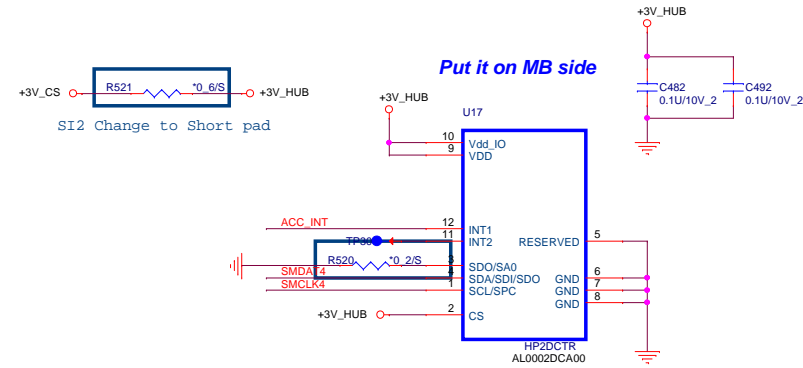
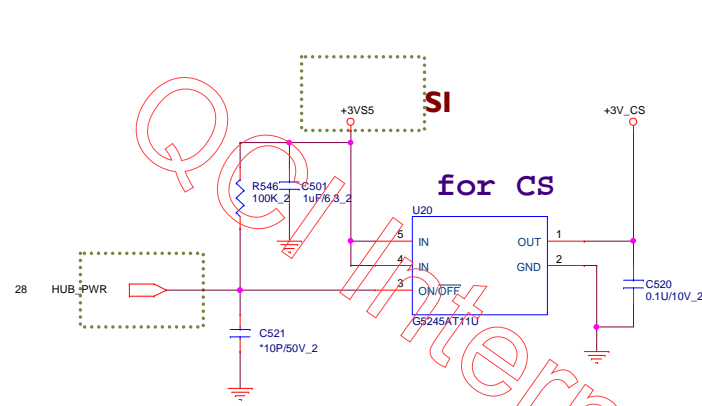


KB backlight

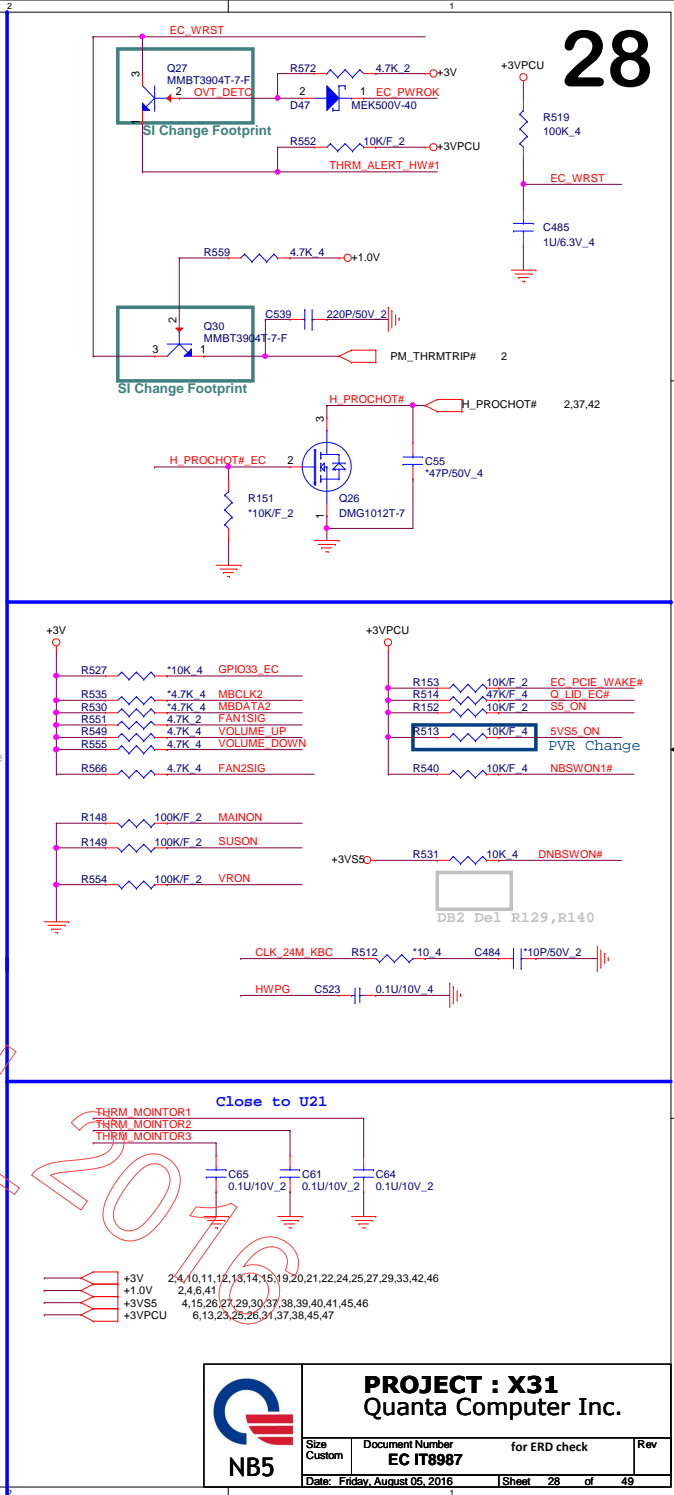
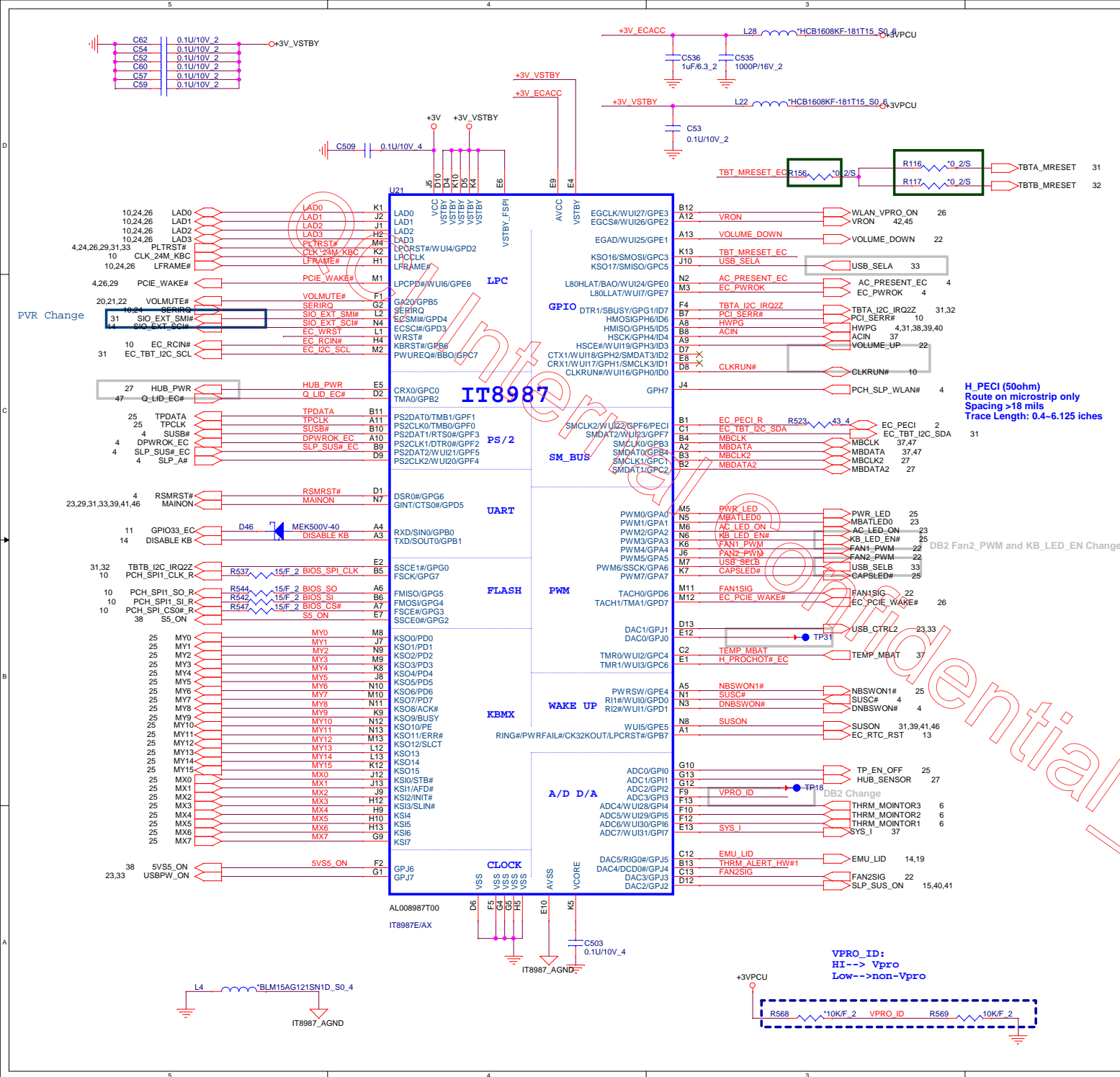
KEYBOARD PULL-UP

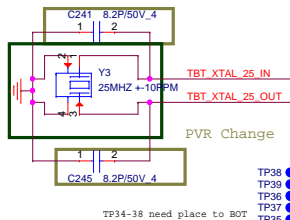


Accelerometer Sensor

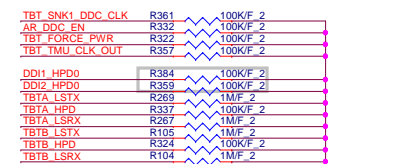
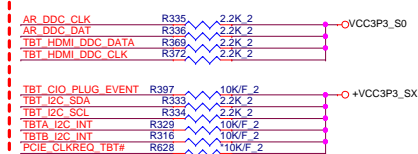
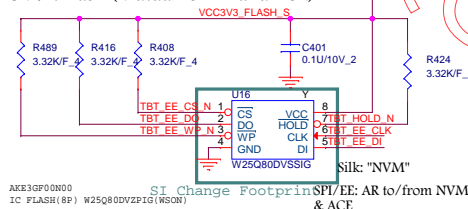
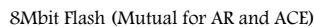


	PROJECT : X31		
	Quanta Computer Inc.		
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		SENSOR HUB	
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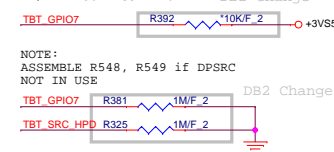




NOTE:
 SNK0_DDC_data/clock?connect to 2k PU only if SRC0 is connected and support HDMI (a.i HDMI or DP++ connector). Otherwise can be 100k PD.
 SNK1_DDC_data?connect to 100k PD. If SRC0 support HDMI, connect as SNK0_CFG1 to GPU and/or appropriate AUX/DDC demux control
 SNK1_DDC_clock?connect to 100k PD.



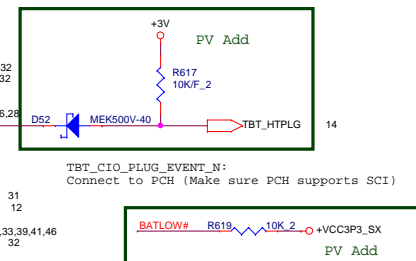
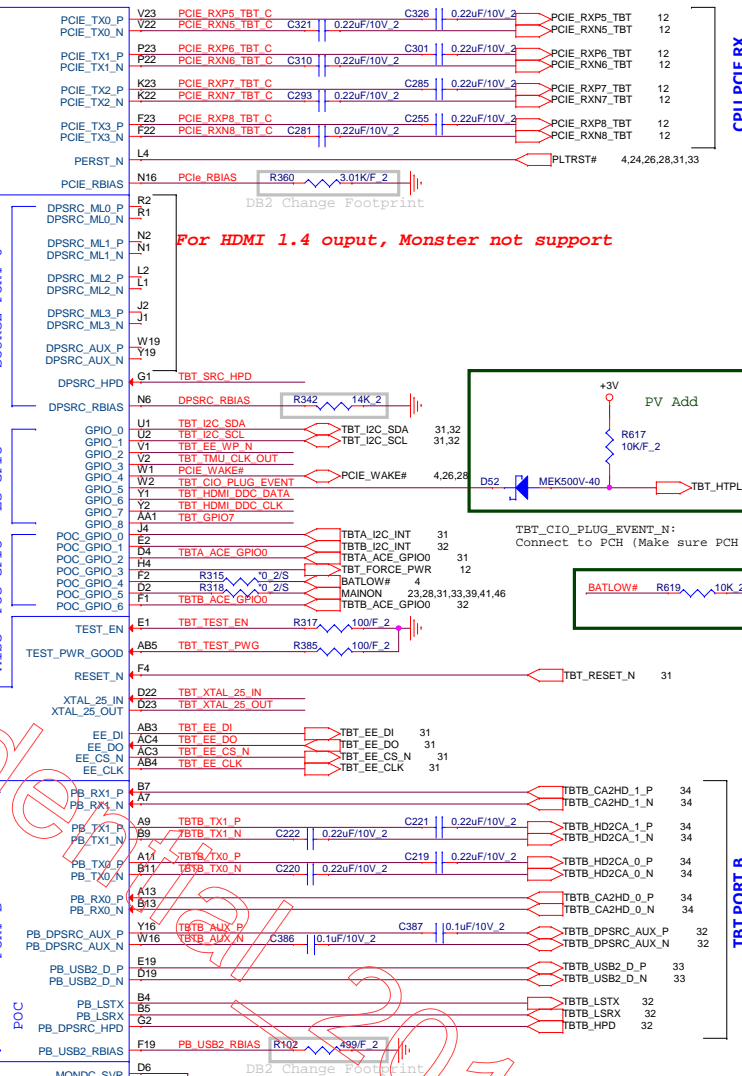
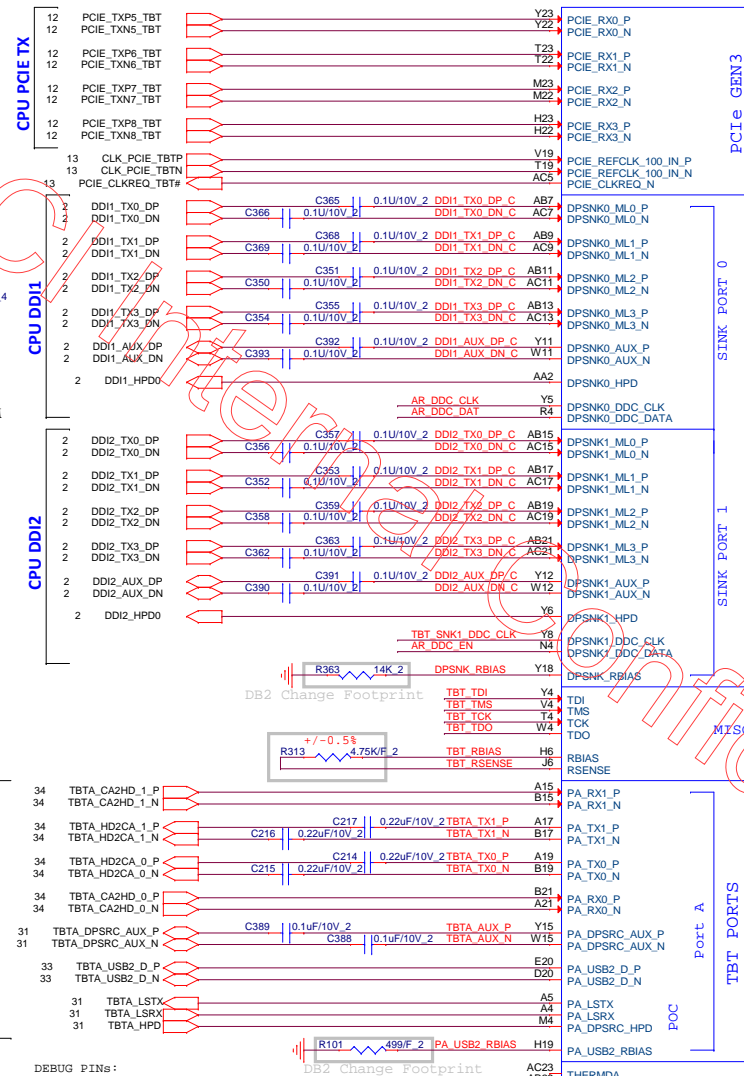
PULL UP - HDMI MODE
DP/HDMI CONFIGURATION DB2 Change



IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

GPIO	TERMINATION	Power Rail
------	-------------	------------

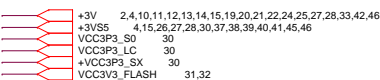
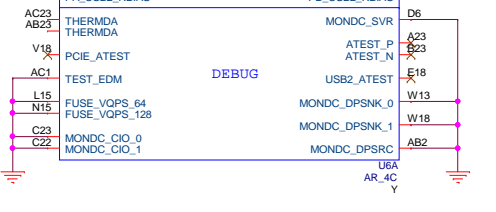
GPIO	TERMINATION	POWER RAIL
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PD	
GPIO_3	100K PD	
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	
GPIO_7	100K PD	
GPIO_8	100K PD	
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PD	
POC_GPIO_3	100K PD	
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	10K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PD	

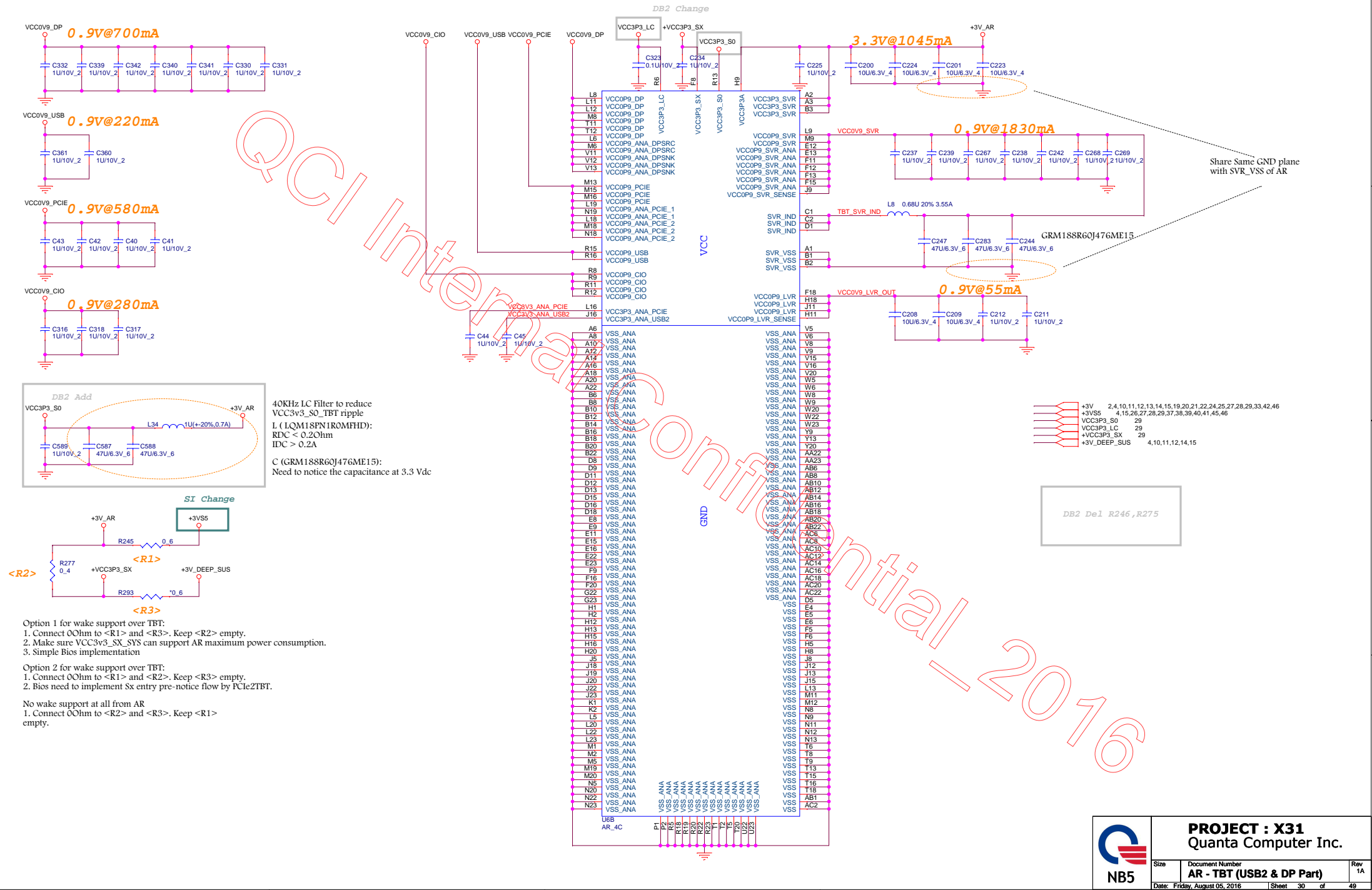


```

DEBUG PINS:
PIN | TERMINATION
-----|-----
MONDC_SVR | GND
MONDC_DPSNK_0 | GND
MONDC_DPSNK_1 | GND
MONDC_DPSRC | GND
MONDC_CIO_0 | GND
MONDC_CIO_1 | GND
TEST_EDM | GND
FUSE_VOPS_64 | GND
FUSE_VOPS_128 | GND
ATEST_P/N | FLOATING
USB2_ATEST | FLOATING
PCIE_ATEST | FLOATING

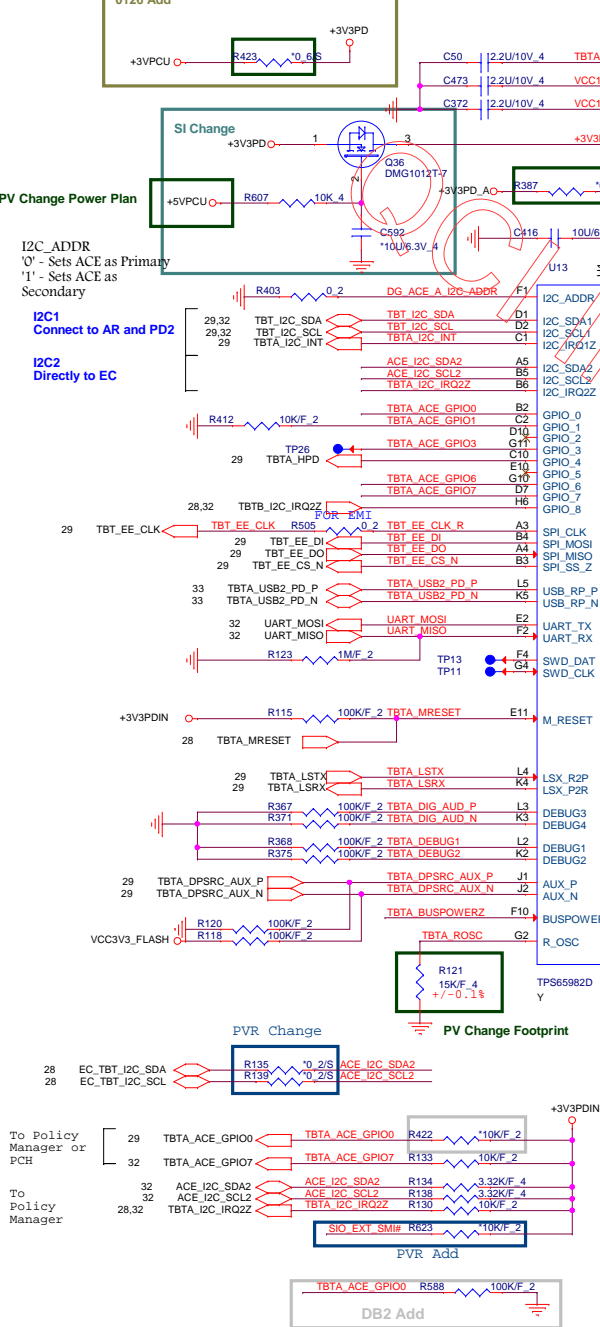
```





Port A Controller - ACE

TPS65982 (ACE) -
USB3.1 PD



31



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Quanta Computer Inc.

Size	Document Number	Rev
NB5	AR - TBT (USB2 & DP Part)	1A
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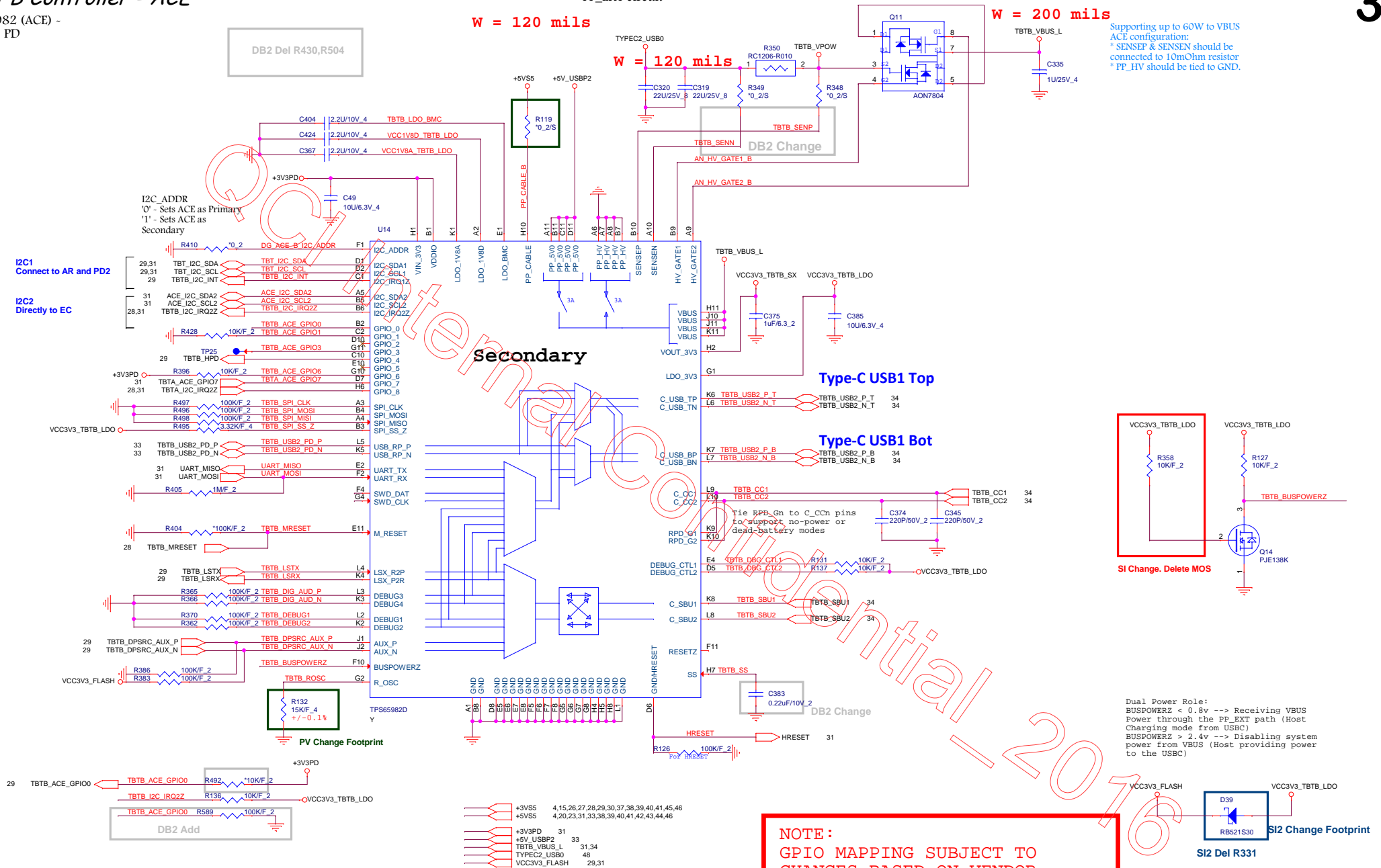
I'm from VIETNAM sualaptop365

Port B Controller - ACE

TPS65982 (ACE) -
USB3.1 PD

PP_EXT circuit

32



Supporting up to 60W to VBUS
ACE configuration:
* SENSEP & SENSEN should be
connected to 10mOhm resistor
* PP_HV should be tied to GND.

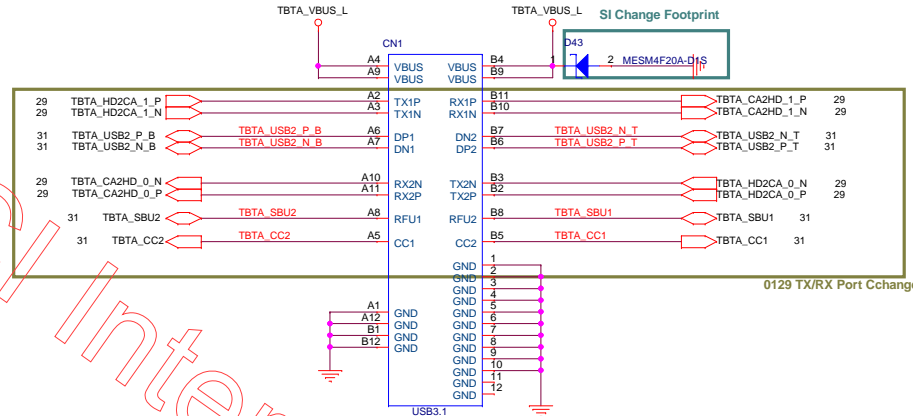
Dual Power Role:
BUSPOWERZ < 0.8v --> Receiving VBUS
Power through the PP_EXT path (Host
Charging mode from USB)
BUSPOWERZ > 2.4v --> Disabling system
power from VBUS (Host providing power
to the USB)



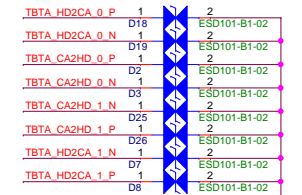
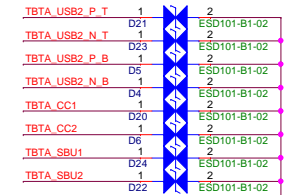
PROJECT : X31
Quanta Computer Inc.

Size	Document Number	Rev
NB5	AR - TBT (USB2 & DP Part)	1A
Date: Friday, August 05, 2016	Sheet 32 of 49	

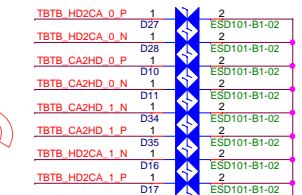
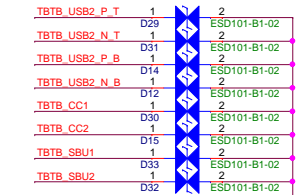
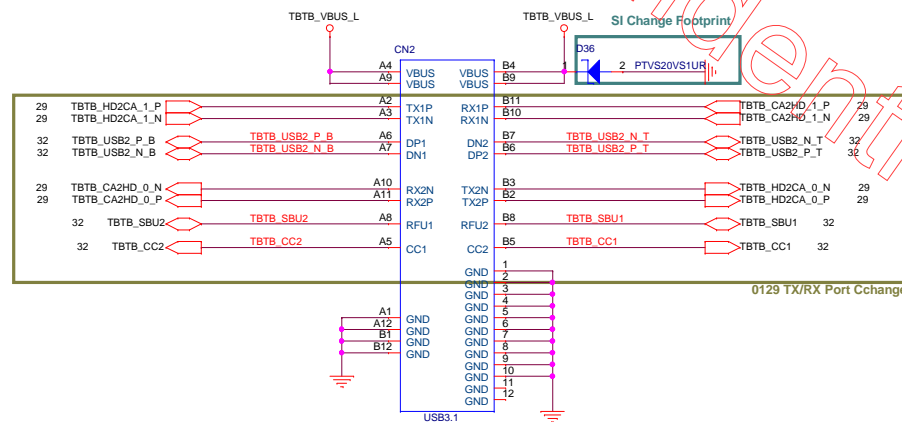
USB Type-C Port A



WAIT ESD FP



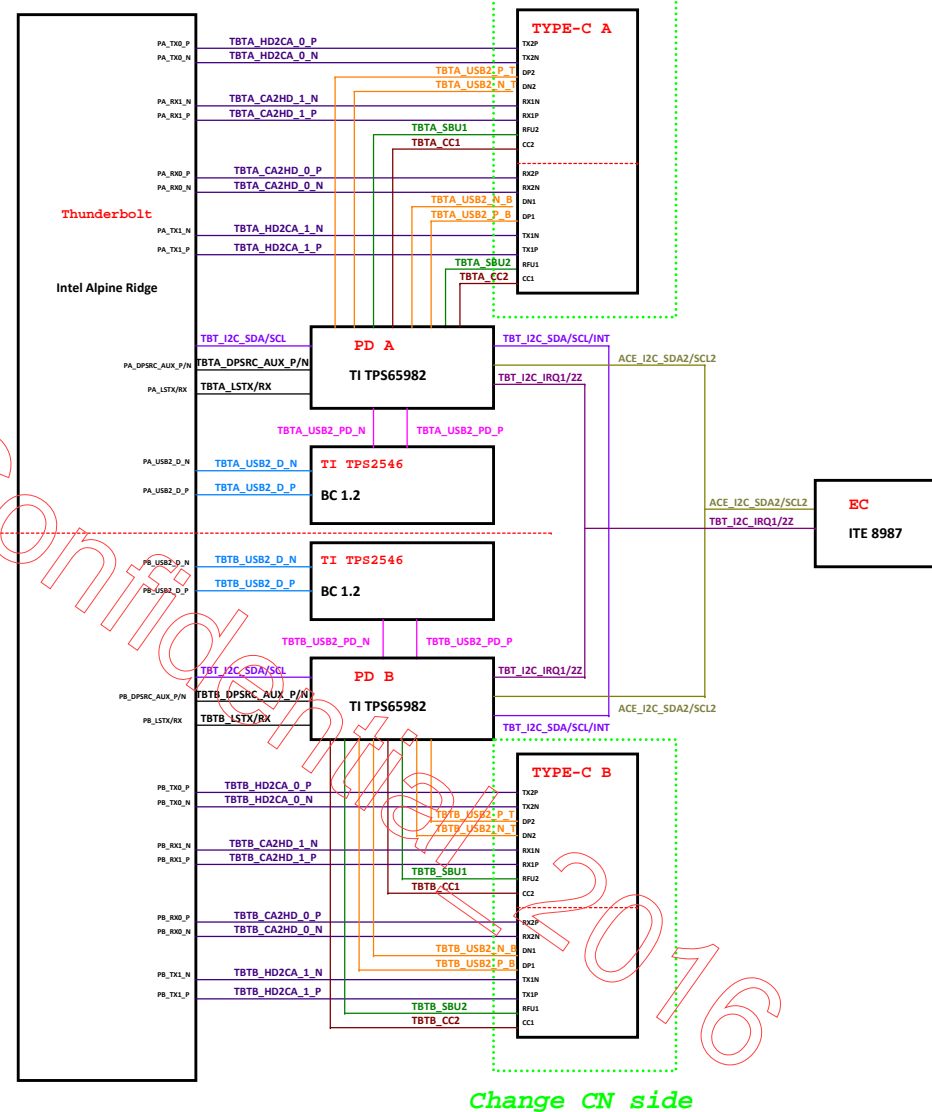
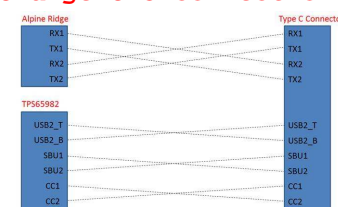
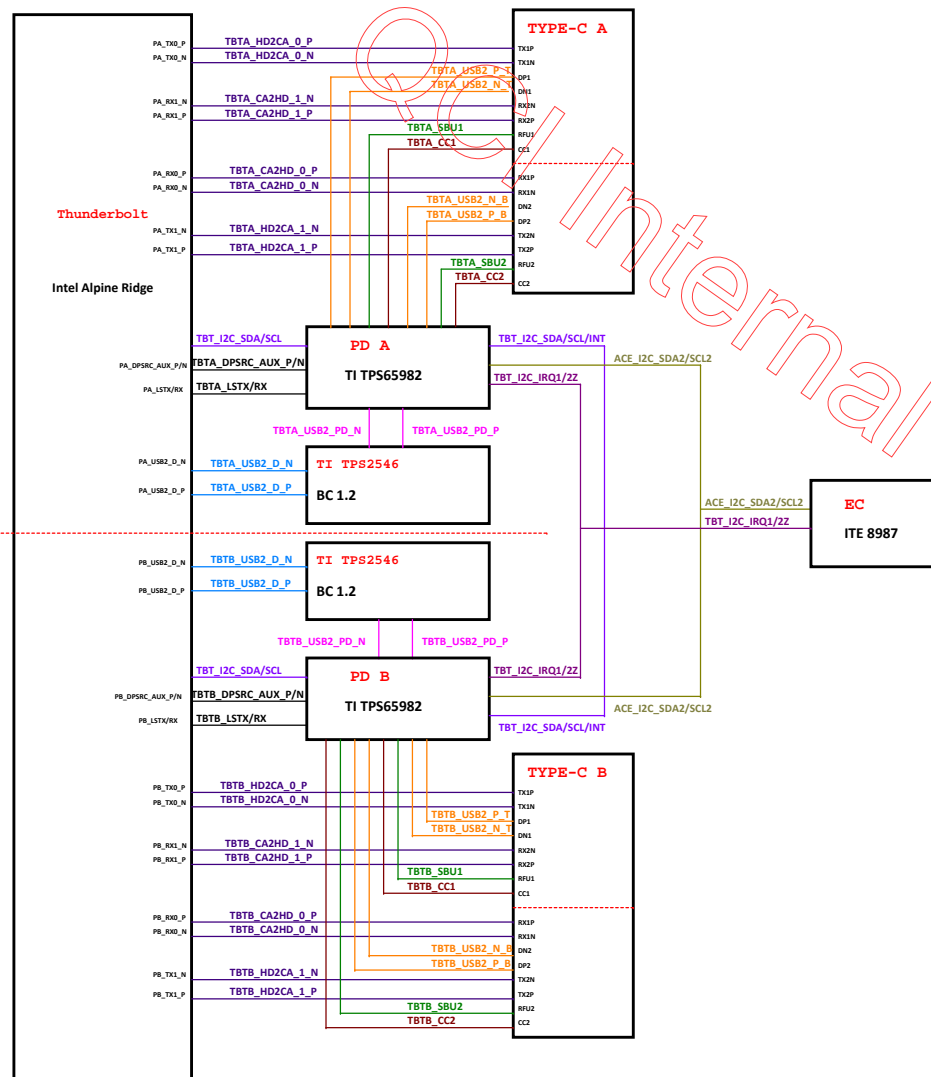
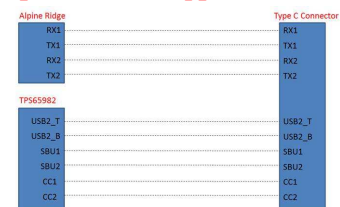
USB Type-C Port B



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Quanta Computer Inc.

Size	Document Number	Rev
NB5	AR - TBT (USB2 & DP Part)	1A
Date: Friday, August 05, 2016	Sheet 34 of 49	

Change CIO connection in Type-C Connector side



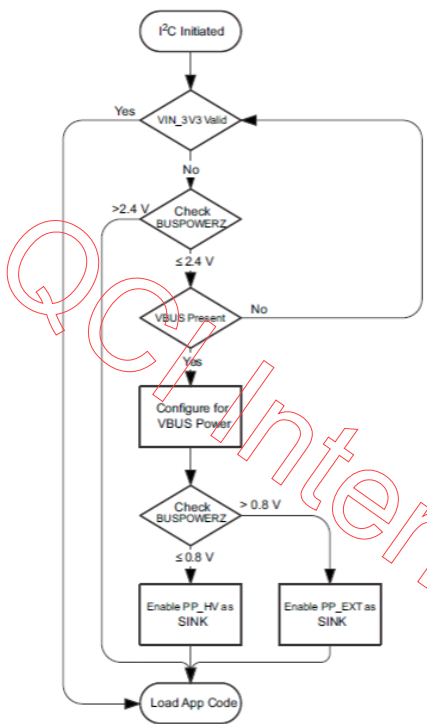


Figure 65. Dead-Battery Condition Flow Diagram

Receptacle (Front View)

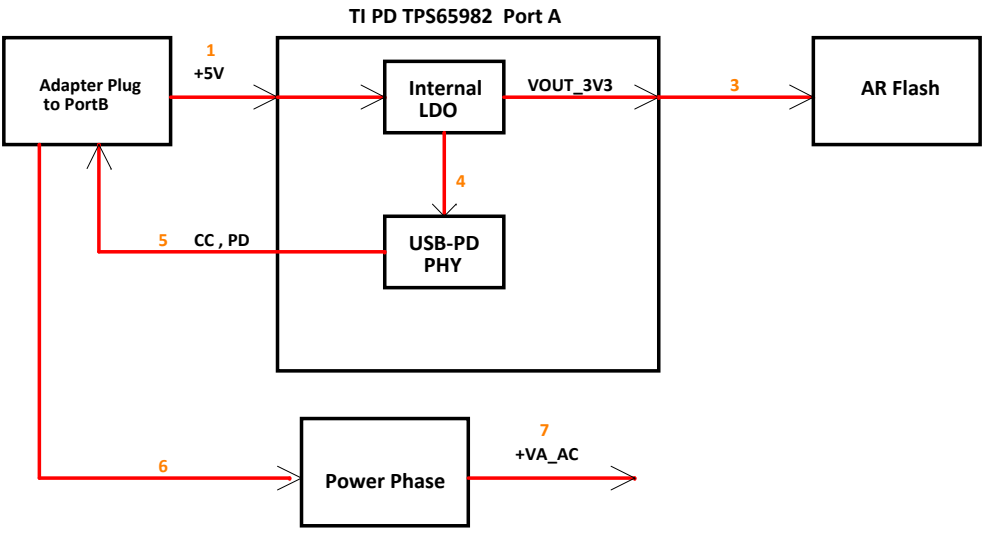
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

USB3.0 USB2.0 USB3.0

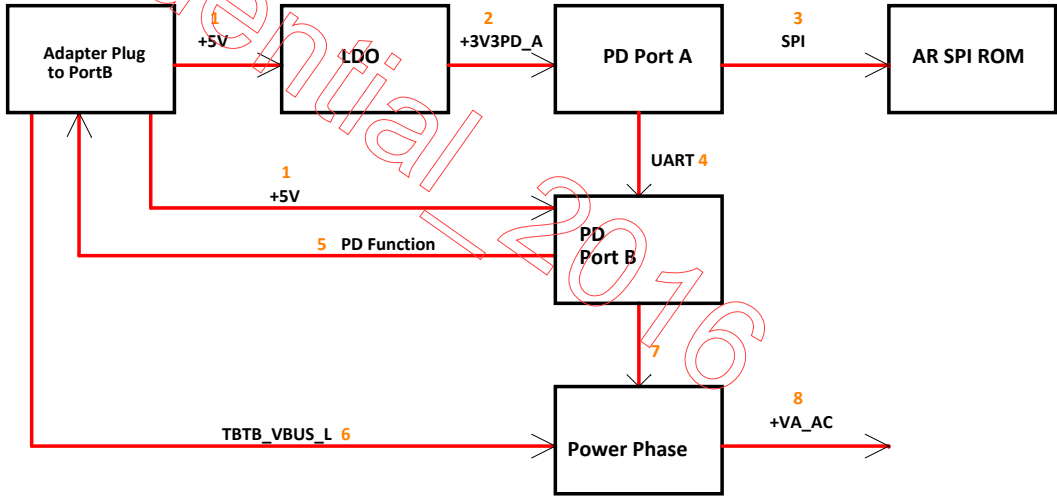
Normal Plug Reverse Plug

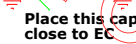
A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2-	VBUS	SBU1	D-	D+	CC	VBUS	TX1-	TX1+	GND
GND	TX2+	TX2-	VBUS	VCONN			SBU2	VBUS	RX1-	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

PortA Dead Battery

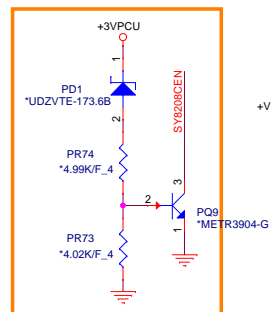
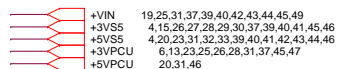


PortB Dead Battery



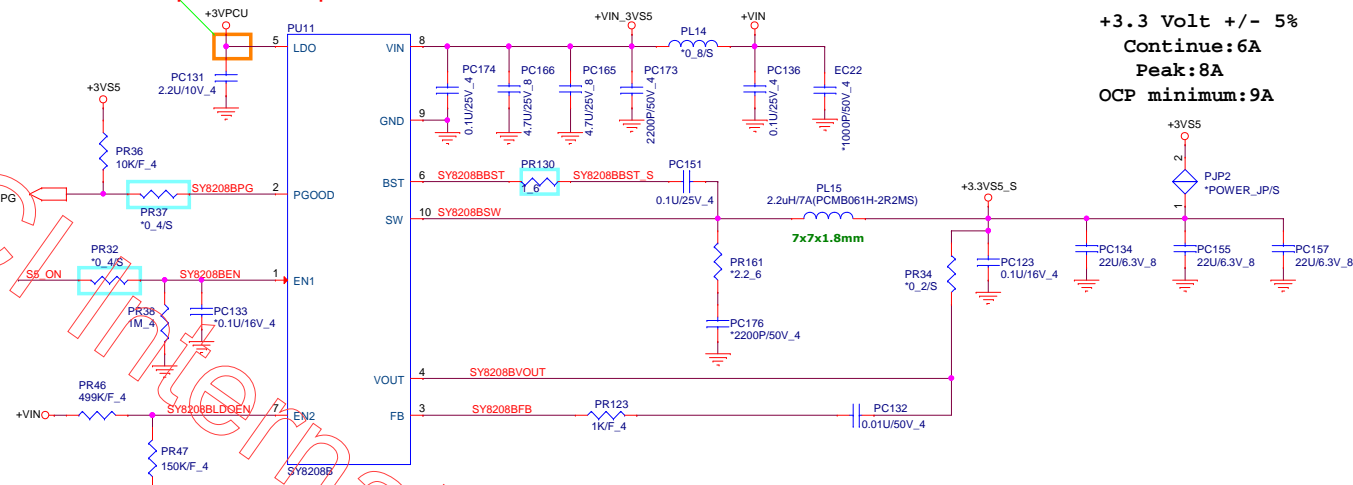


Size Custom	Document Number Charger(ISL9237)	Rev 1A
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2014/12/12 updated

Do Not add test pad on VCC & LDO pin



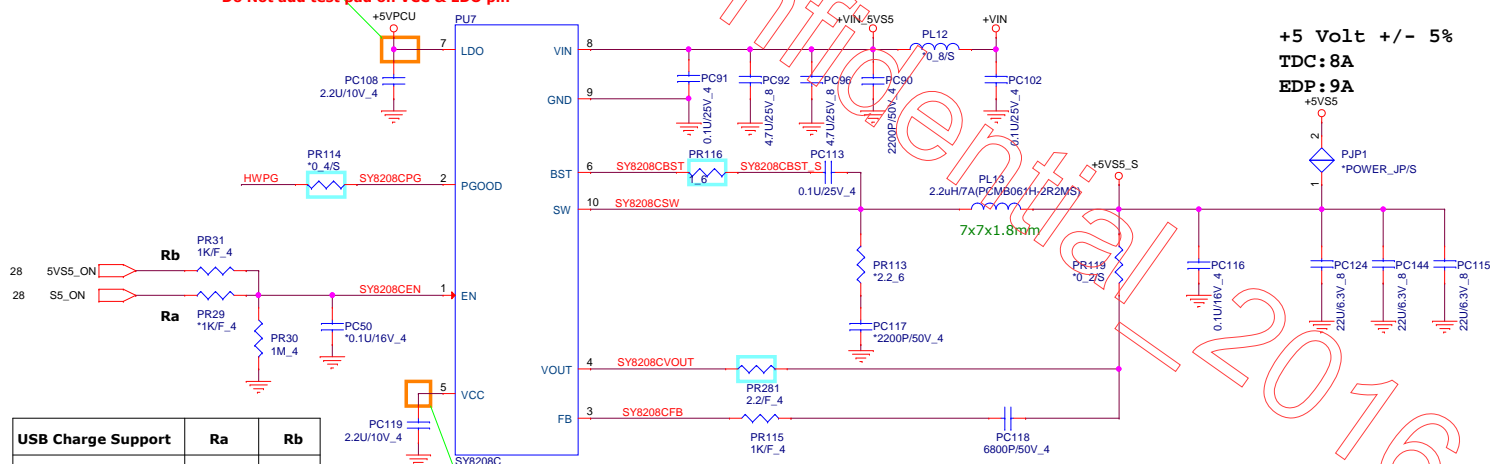
+3.3 Volt +/- 5%

Continue: 6A

Peak: 8A

OCP minimum: 9A

Do Not add test pad on VCC & LDO pin



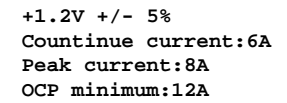
+5 Volt +/- 5%

TDC:8A

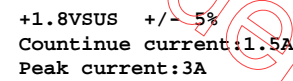
EDP: 9A

USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

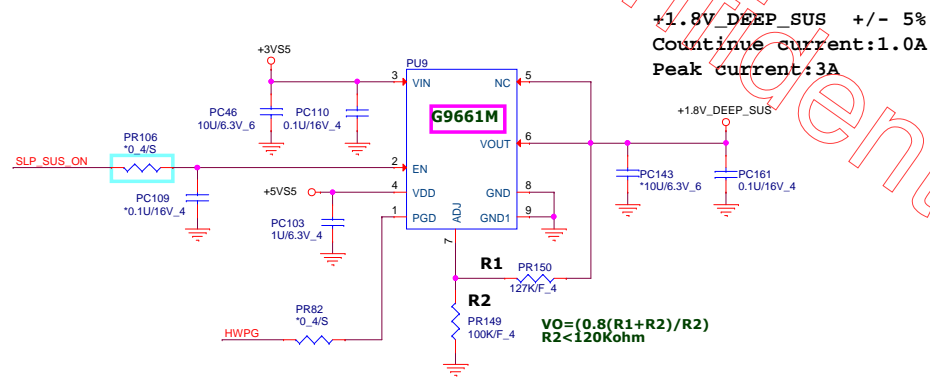
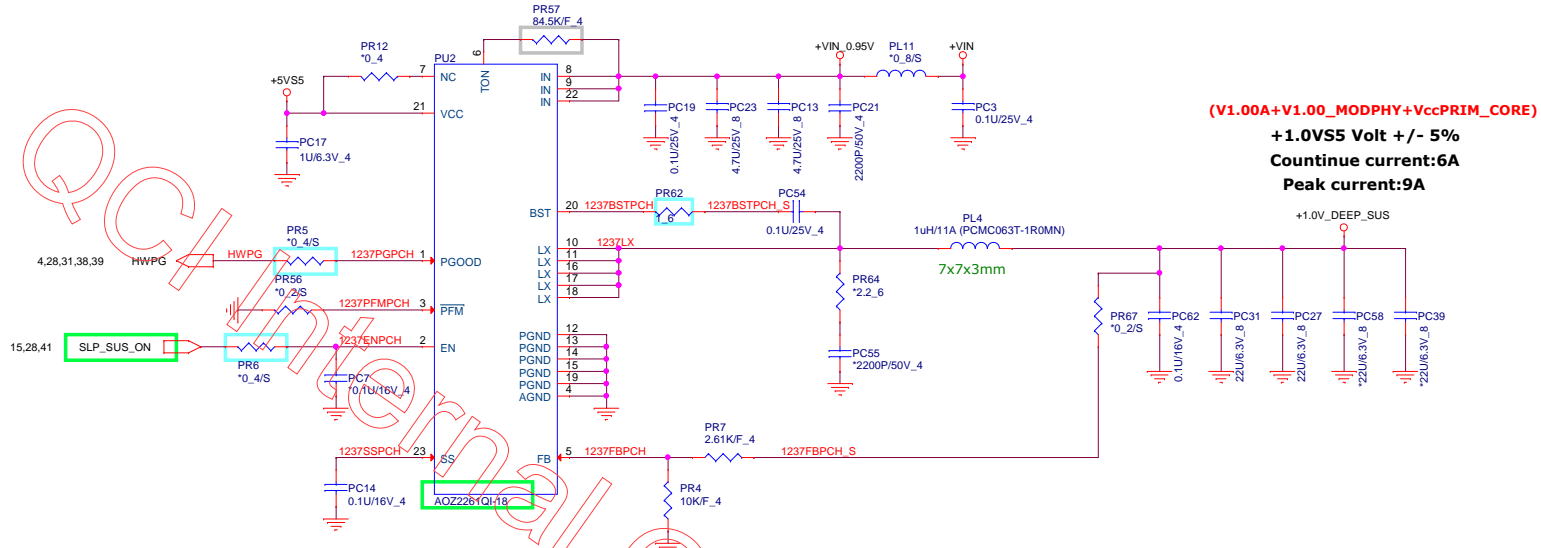
Do Not add test pad on VCC & LDO pin



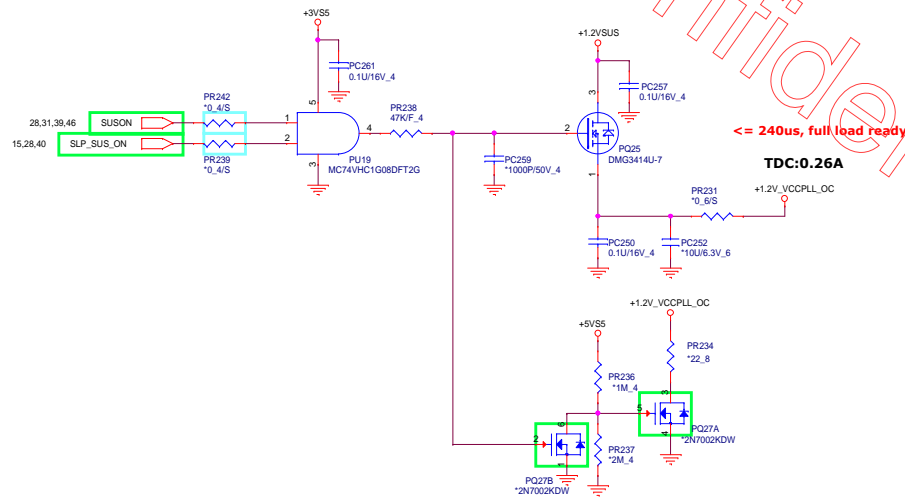
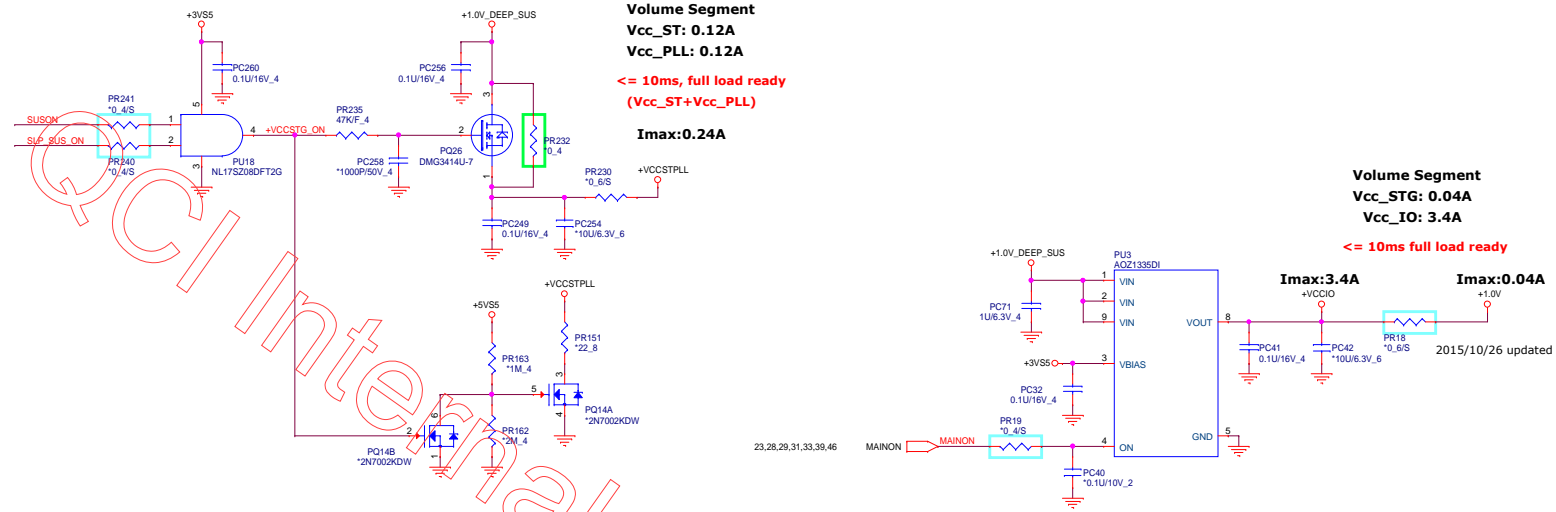
	S3	S5	+1.2VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

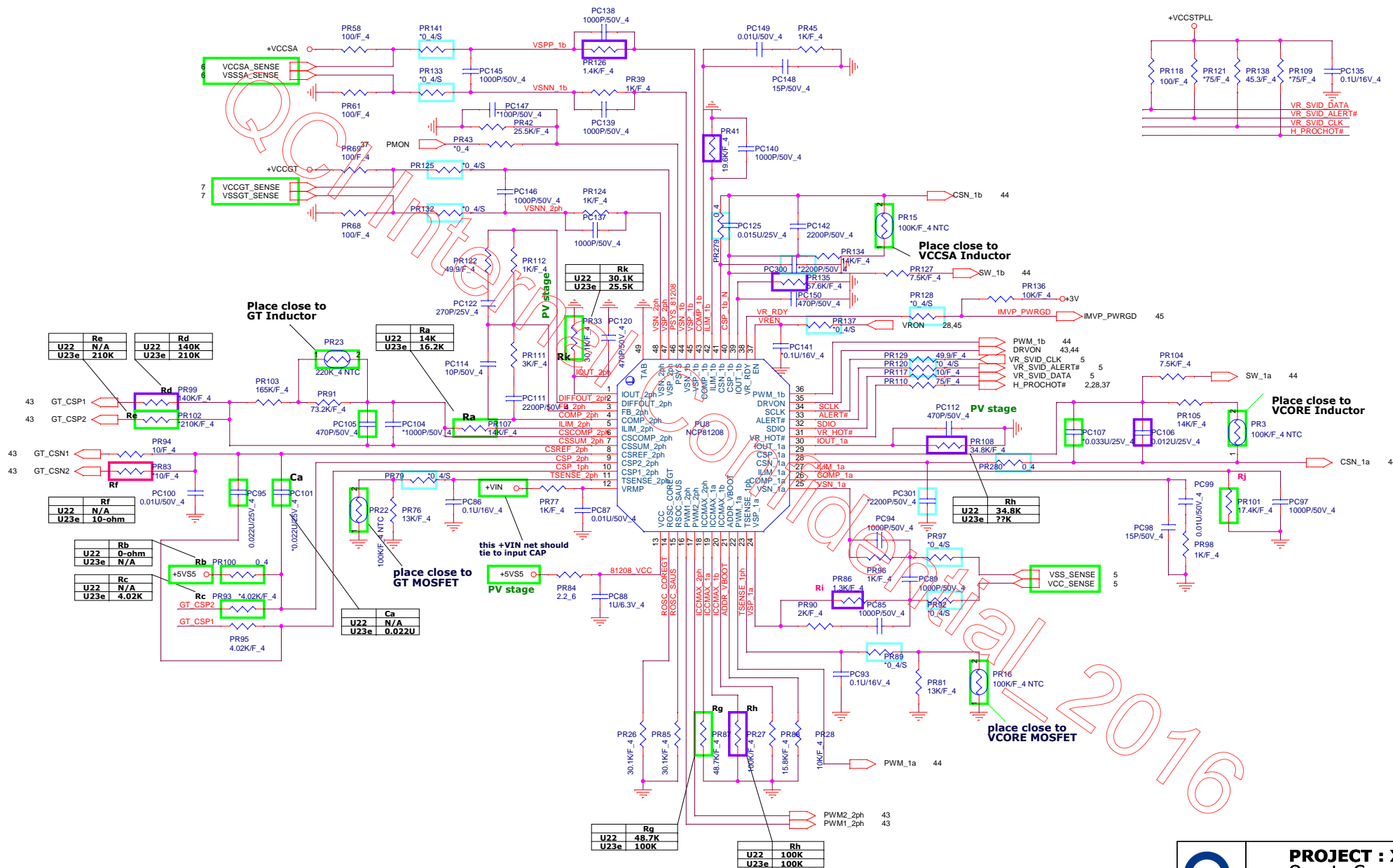


+VIN 19,25,31,37,38,39,42,43,44,45,49
 +3VS5 4,15,26,27,28,29,30,37,38,39,41,45,46
 +5VS5 4,20,23,31,32,33,38,39,41,42,43,44,46
 +1.0V_DEEP_SUS 9,13,15,41
 +1.8V_DEEP_SUS 9,15,37,46



+1.0V	2,4,6,28
+3VSS	4,15,26,27,28,29,30,37,38,39,40,45,46
+5VSS	4,20,23,31,32,33,38,39,40,42,43,44,46
+VCCIO	2,6
+1.2V _{SUS}	3,6,16,17,18,39
+VCCSTPLL	2,5,6,9,42
+1.0V _{DEEP_SUS}	9,13,15,40
+1.2V _{VCCPLL_OC}	6



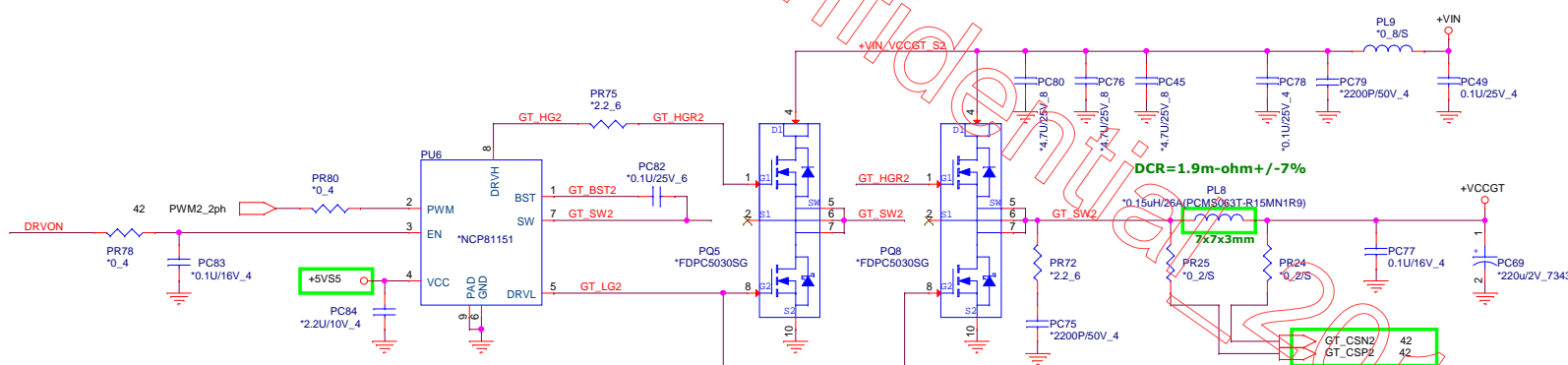


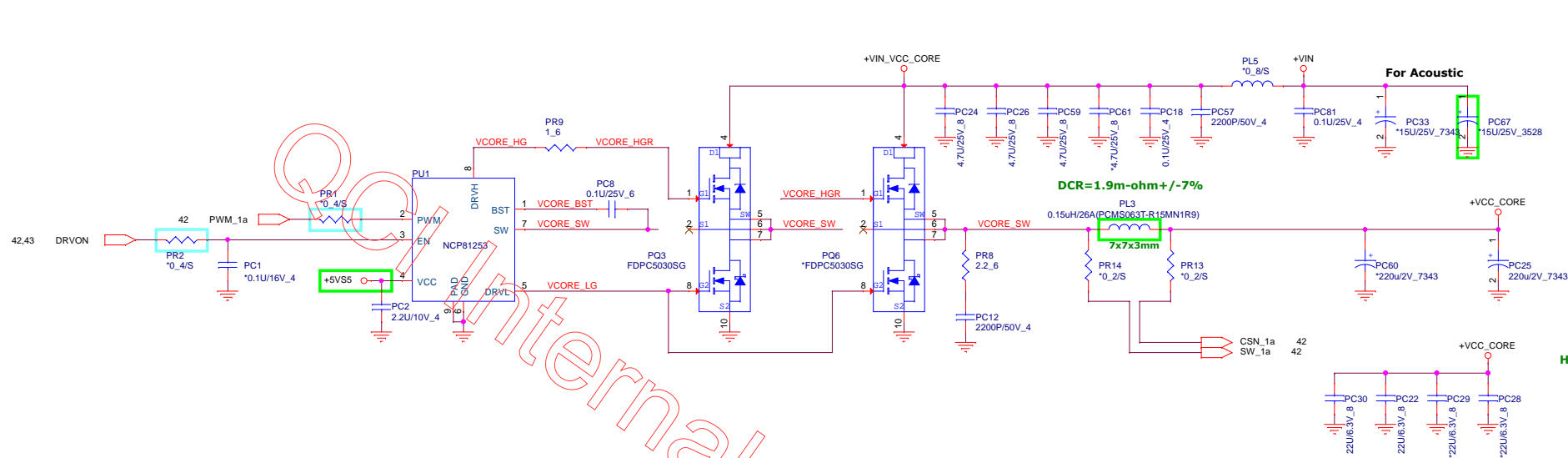


U-line 22 (15W)
TDC:18A(22)
Icc max:31A(22)
L/L=3.1mV/A

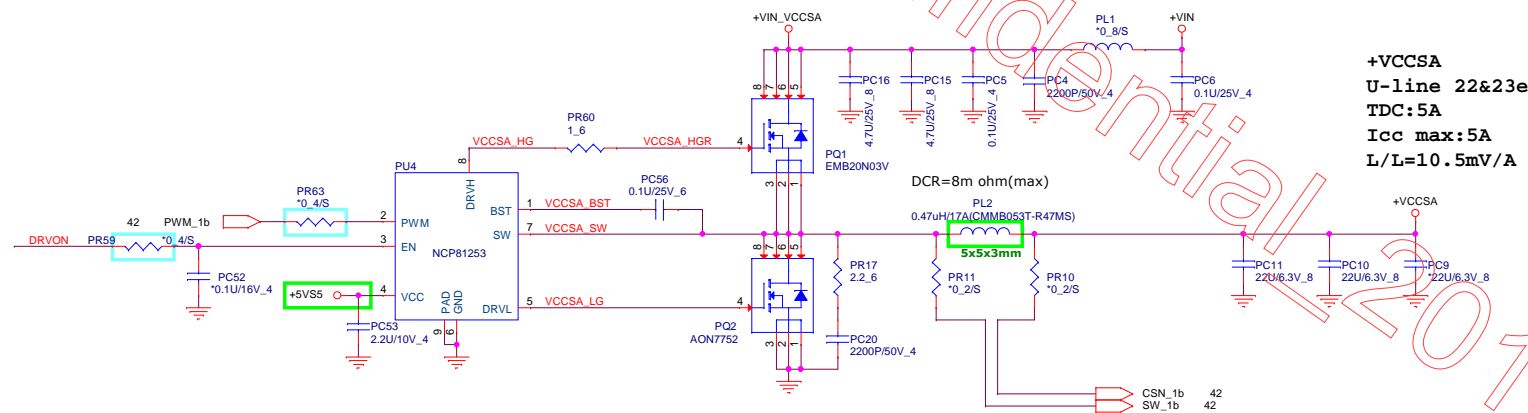
U-line 23e(28W)
TDC:35A(23e)
Icc max =64A(GT+GTx)
L/L=2mV/A

47U/6.3V_0805 X 6
22U/6.3V_0603 X 12 (GTX+5)
10U/6.3V_0402 X 10
1U/6.3V_0402 X 12

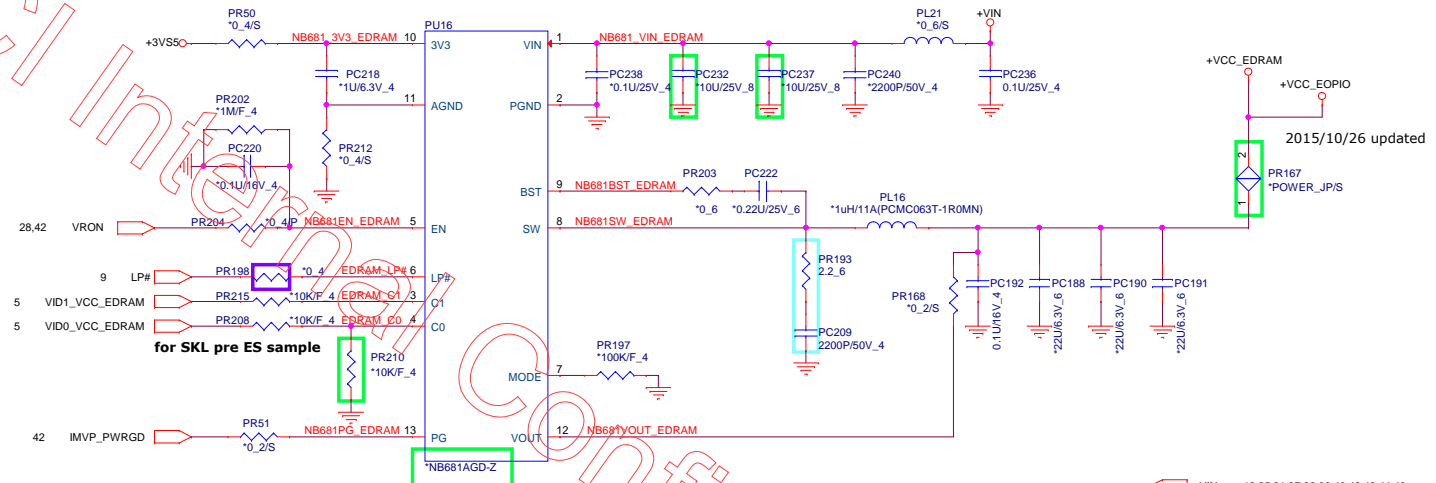
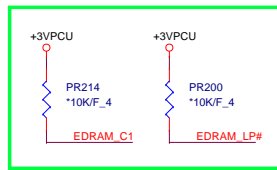




VCCSA



+VCC_EDRAM +/- 5%
 Countinue current:4.5A
 Peak current:6A



VCC_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

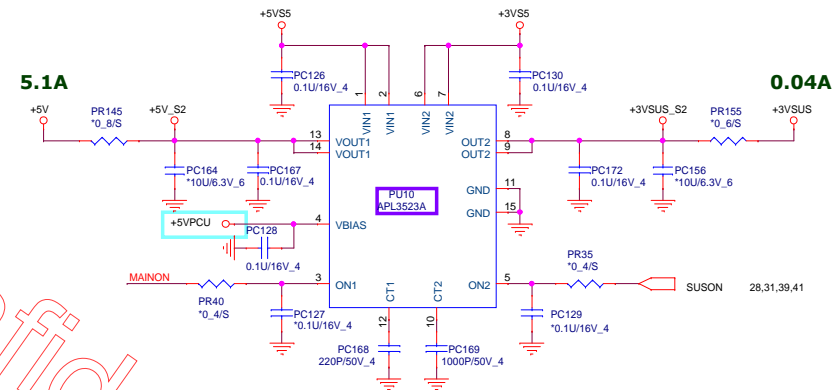
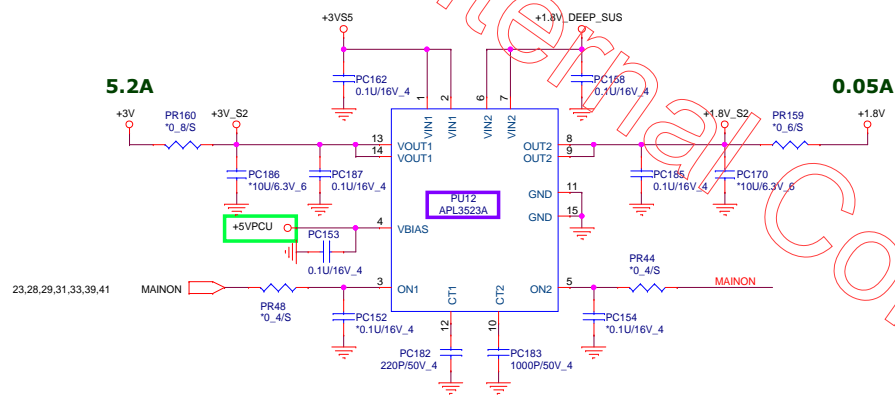
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 +3VS5 4,15,26,27,28,29,30,37,38,39,40,41,46
 +3VPCU 6,13,23,25,26,28,31,37,38,47
 +VCC_EOPIO 5
 +VCC_EDRAM 5

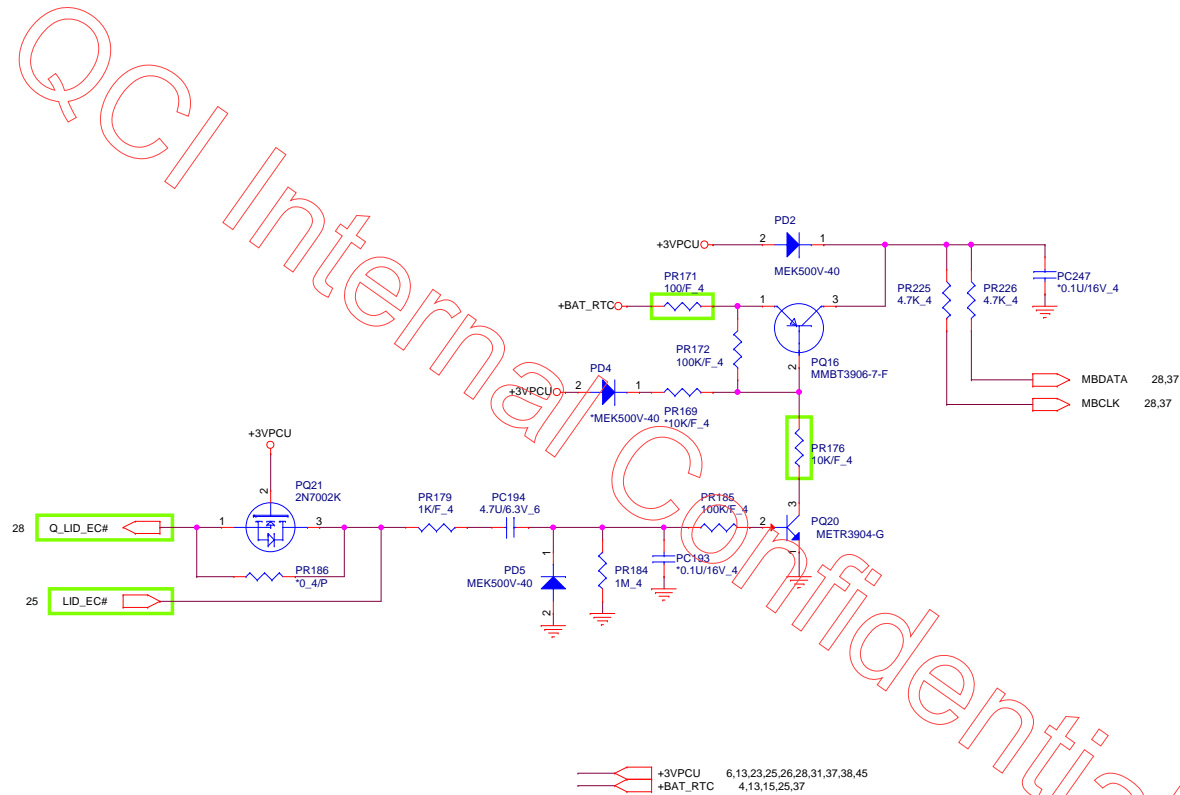


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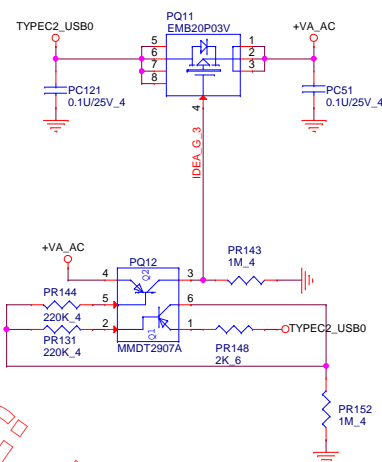
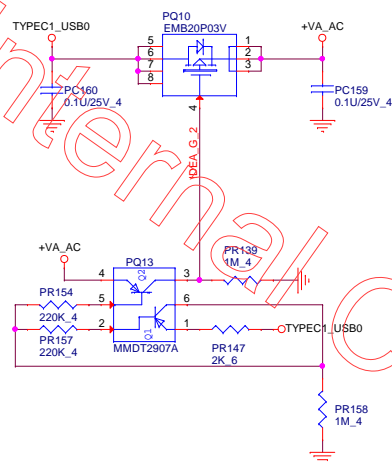
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+3V	2,4,10,11,12,13,14,15,19,20,21,22,24,25,27,28,29,33,42
+5V	20,21,22,25
+1.8V	5,20,21
+3VS5	4,15,26,27,28,29,30,37,38,39,40,41,45
+5VS5	4,20,23,31,32,33,38,39,40,41,42,43,44
+3VSUS	25,26
+5VPCU	20,31,38

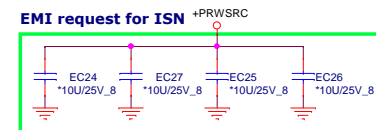
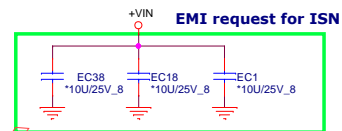





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TYPE1_USB0 31
TYPE2_USB0 32



		PROJECT : X31	
		Quanta Computer Inc.	
Size Custom	Document Number TYPE C S/W	Rev 1A	
Date: Friday, August 05, 2016	Sheet 48 of 49		



+VIN 19,25,31,37,38,39,40,42,43,44,45
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	Size Custom	Document Number EMI solution
Date: Friday, August 05, 2016		Sheet 49 of 49